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Analysis of Transformerless Single-Phase Inverters in PV Grid-Connected Application

TESI DI LAUREA MAGISTRALE IN
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Abstract

Photovoltaic (PV) systems are now widely integrated into the electric grid due to the growing need for renewable energy. Transformerless topologies have drawn interest among the various inverter layouts utilized in PV applications because of their increased efficiency, reduced cost, and small size. Nonetheless, a significant issue with transformerless systems is the creation of leakage current due to common-mode voltage fluctuations, which may compromise grid compliance and safety.

This thesis focuses on the analysis and comparison of two transformerless single-phase inverter topologies that have been studied extensively: HERIC and H5 for PV grid-connected applications. The primary objective is to reduce leakage current by improving system performance and lowering common-mode voltage swings. Both topologies transitory states and switching behavior are carefully investigated. In the context of the H5 inverter, the effect of junction capacitance on transient behavior is also examined.

Additionally, a modulation method is suggested to improve both inverter types reactive power capabilities, allowing them to function in non-unity power factor scenarios and guaranteeing adherence to contemporary grid requirements. The efficiency of the suggested strategies in lowering leakage current and enhancing inverter performance is validated by simulation results.

The study's conclusions aid in the development of transformerless PV inverters that are safer and more effective for use in actual grid-connected applications.

Keywords:

Transformerless inverter, HERIC, H5, PV-grid connection, leakage current, common-mode voltage, reactive power, modulation technique, junction capacitance.

Abstract in lingua italiana

Sistemi fotovoltaici (PV) sono ormai ampiamente integrati nella rete elettrica a causa della crescente necessità di energia rinnovabile. Le topologie senza trasformatore hanno suscitato interesse tra i vari layout di inverter utilizzati nelle applicazioni fotovoltaiche per la loro maggiore efficienza, il costo ridotto e le dimensioni contenute. Tuttavia, un problema significativo nei sistemi senza trasformatore è la generazione di corrente di dispersione dovuta alle fluttuazioni della tensione di modo comune, che può compromettere la conformità alla rete e la sicurezza.

Questa tesi si concentra sull'analisi e il confronto di due topologie di inverter monofase senza trasformatore ampiamente studiate: HERIC e H5 per applicazioni fotovoltaiche connesse alla rete. L'obiettivo principale è ridurre la corrente di dispersione migliorando le prestazioni del sistema e riducendo le variazioni della tensione di modo comune. Gli stati transitori e il comportamento di commutazione di entrambe le topologie sono analizzati attentamente. Nel contesto dell'inverter H5, viene inoltre esaminato l'effetto della capacità di giunzione sul comportamento transitorio.

Inoltre, viene proposta una tecnica di modulazione per migliorare la capacità di gestione della potenza reattiva di entrambi i tipi di inverter, consentendo il funzionamento in scenari con fattore di potenza non unitario e garantendo la conformità agli attuali requisiti di rete. L'efficacia delle strategie proposte nella riduzione della corrente di dispersione e nel miglioramento delle prestazioni degli inverter è convalidata dai risultati delle simulazioni.

Le conclusioni dello studio contribuiscono allo sviluppo di inverter fotovoltaici senza trasformatore più sicuri ed efficienti per l'impiego in applicazioni reali connesse alla rete.

Parole chiave:

Inverter senza trasformatore, HERIC, H5, connessione FV-rete, corrente di dispersione, tensione di modo comune, potenza reattiva, tecnica di modulazione, capacità di giunzione.

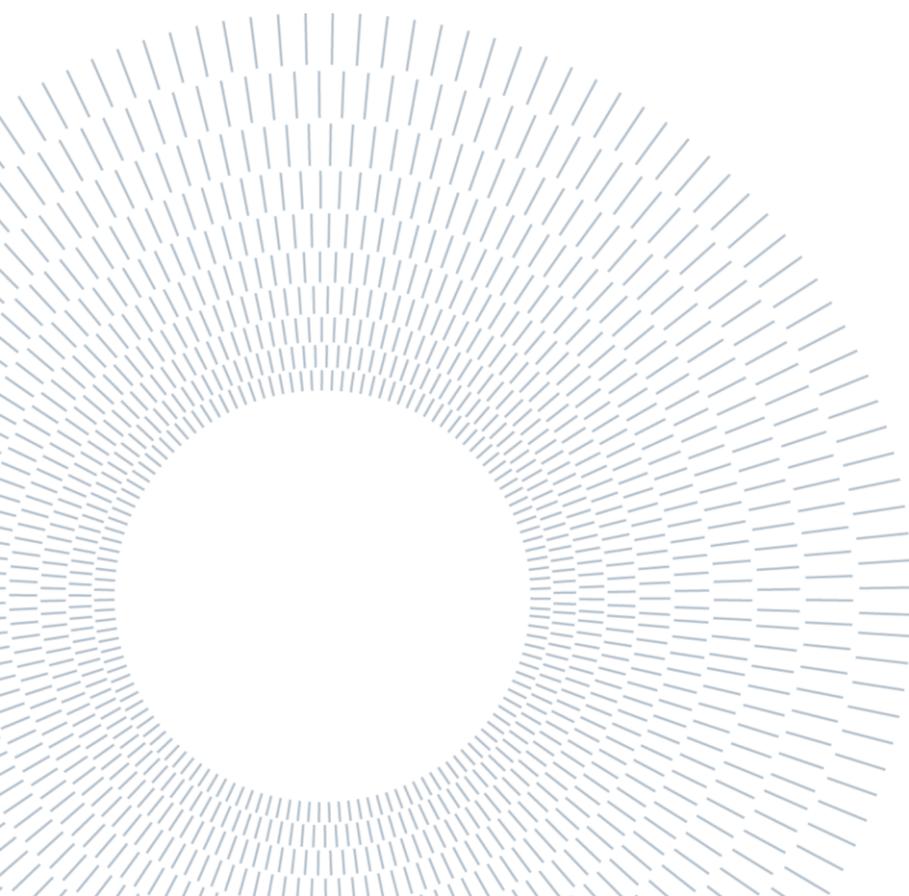
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Introduction

The global demand for clean energy has risen, while the traditional fossil fuel-based resources are finite and environmentally unsustainable. As a result, the solar photovoltaic (PV) energy has emerged as a promising alternative. They are environmentally friendly, producing no emissions, noise, or waste products during operation. With no moving parts, PV systems require minimal maintenance and have long operational lifetimes of up to 30 years.

Solar photovoltaic (PV) panels used for electric power generation are not directly connected to the grid. This is because of differences in the type of power generated and the power required by both the solar panels and the grid. In the past, power electronic converters were designed with small to large transformers, which led to many challenges of weight, cost, size, and reduced efficiency. With the recent advances in technology, the design of transformerless PV inverters evolved in order to address the existing challenges.

A major challenge in grid-connected PV systems with transformerless inverters is leakage current. The leakage current flowing through the parasitic capacitance of the photovoltaic array and the grid result in severe voltage fluctuations.

This thesis investigates two transformerless inverter topologies HERIC and H5 for single-phase PV grid-connected applications. The main goal is to suppress leakage current by minimizing common-mode voltage variation and to achieve better performance than the conventional full-bridge inverter. The work includes a detailed analysis of each inverter's switching states and transient behaviors, as well as the impact of junction capacitance on system performance. Additionally, a modulation technique is proposed to enhance the reactive power capability of both topologies, improving their compliance with modern grid standards.

The study begins as follows. Chapter 1 presents an overview of PV-grid connected systems, the role of inverters, and the motivation for transformerless designs.

Chapter 2 describes the main inverter components and the control system.

Chapter 3 introduces the conventional full-bridge inverter to provide a reference baseline for comparison with the HERIC and H5 transformerless topologies in later chapters.

Chapter 4 analyzes the structure and operating principles of the HERIC inverter, with a focus on switching transitions and leakage current behavior. Chapter 5 presents a detailed study of the H5 inverter, including an enhanced version and the influence of junction capacitance during transient states. Finally, chapter 6 explores the reactive

power capability of both topologies and introduces a proposed modulation method to enable non-unity power factor operation.

1. Overview of grid connected PV systems

1.1 Photovoltaic Inverters

The photovoltaic systems that are connected to the low-voltage grids are an essential part of the distributed generation networks. One of the major challenges of increasing the usage of the PV systems is the cost-effectiveness, complexity and the lightweight design that be suitable for the residential applications, also, ensuring the safety for human interaction and high reliability compatible with PV panel. The modern design of inverters has been developed to enhance the suitable cost by considering the efficiency of photovoltaic systems. A comprehensive categorization of the types of inverters connected to the grid is shown in Figure 1.1 [1].

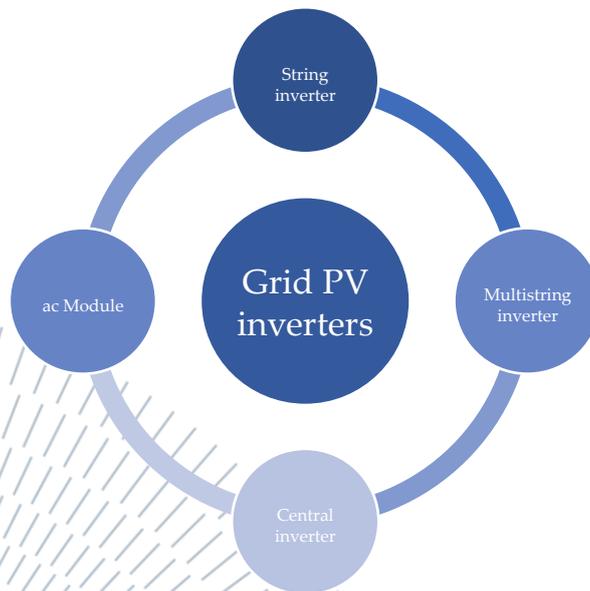


Figure 1.1: PV inverter classifications

1.1.1 Central inverters

In photovoltaic systems that has capacities more than 10kWp modules are typically connected in parallel strings to a single central inverter as shown in Figure 1.2(a). In the past, systems used thyristor-based line-commutated inverters that have been replaced by more efficient and cost-effective IGBT-based force-commutated inverters. However, central inverter systems have several limitations, including [2]:

- The need for long high-voltage DC cables
- Reduced efficiency due to centralized MPPT
- Energy loss from mismatch between PV modules
- Diode-related power losses in strings
- Reduced system reliability due to dependence on a single inverter.

1.1.2 String inverters

String inverters, developed in Europe around 1995 as shown in Figure 1.2(b). in this kind of inverter each PV string connects to its own inverter. These inverters operate in parallel and feed into the grid. If the string voltage is suitable, no voltage improving is required, enhancing efficiency. In comparison to central inverters, they have many advantages [2]:

- No losses from string diodes
- Individual MPPT for each string
- Higher overall energy yield
- Lower cost due to large-scale production

1.1.3ac Modules inverters

AC modules inverters consist of individual solar panels each paired with its own inverter and MPPT unit as shown in Figure 1.2(c). This configuration removes mismatch losses and optimizes power output per panel. Its modular “plug & play” nature allows the growth of the system easier. However, the total efficiency is slightly lower due to high-voltage improving, and the cost per watt remains high. However, mass production is expected to reduce this over time.

1.1.4 Multi-string inverter

Multi-string inverters, shown in Figure 1.2(d), are a hybrid between string and module inverters. Each photovoltaic string is connected through a specific DC-DC converter with its own MPPT, all feeding into a shared DC-AC inverter. This configuration

enables strings of different sizes, technologies, or orientations to operate efficiently with a single grid-connected inverter [3].

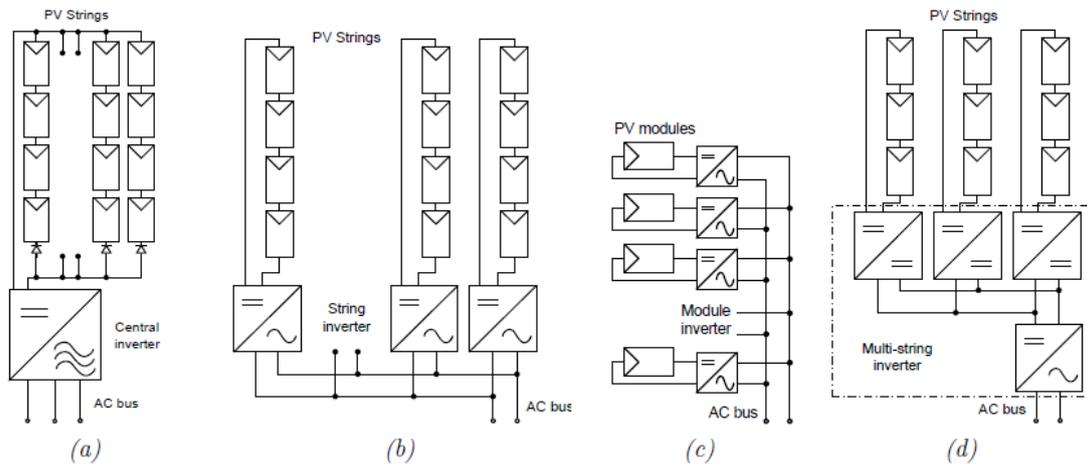


Figure 1.2: Different grid-connected PV inverter structures: Central inverter (a); String inverter (b); Module inverter (c) and Multistring inverter (d)

1.2 Transformerless inverter

Photovoltaic (PV) inverters use on the DC side a high-frequency transformer and on the AC side a line-frequency transformer to provide electrical isolation. The major function of these transformers is to prevent DC current that is injected into the grid from the solar array and to ensure the safety and power quality standards.

Galvanic isolation requirements in grid-connected PV systems depend on local regulations. It is required in some countries like the UK and Italy, and usually achieved with either a low-frequency transformer on the AC side or a high-frequency transformer on the DC side, as shown in Figures 1.3 (a) and (b).

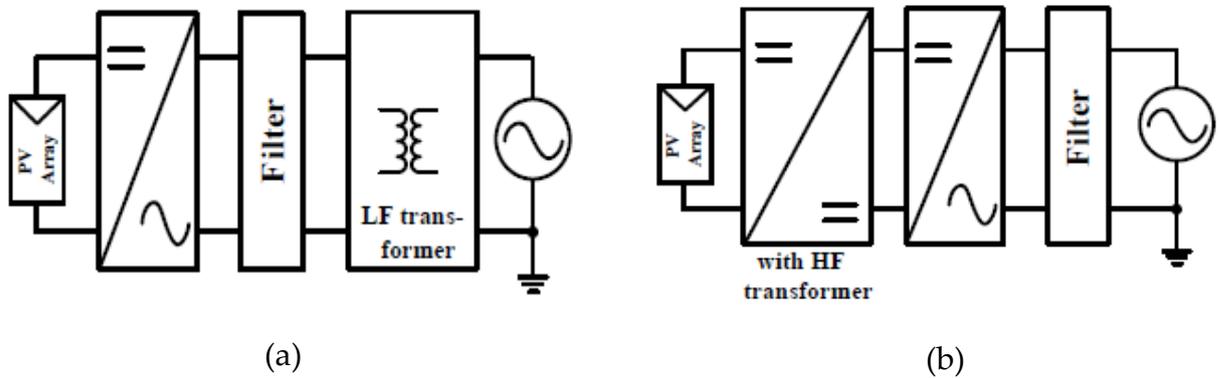


Figure 1.3: Grid-connected PV system using an inverter with galvanic isolation: grid-side low-frequency (LF) transformer (a) or DC side high-frequency (HF) transformer (b)

Besides the advantage of galvanic isolation in the PV systems, it includes some drawbacks such as increased size, weight, and cost, difficulties for installations, and reduced efficiency.

In some countries, like Spain and Germany, galvanic isolation is not obligatory. So, the transformer can be removed, and the other technological methods are used to ensure separation between the PV array and the electrical grid. Figure 1.4 illustrates the configuration of a transformerless PV system.

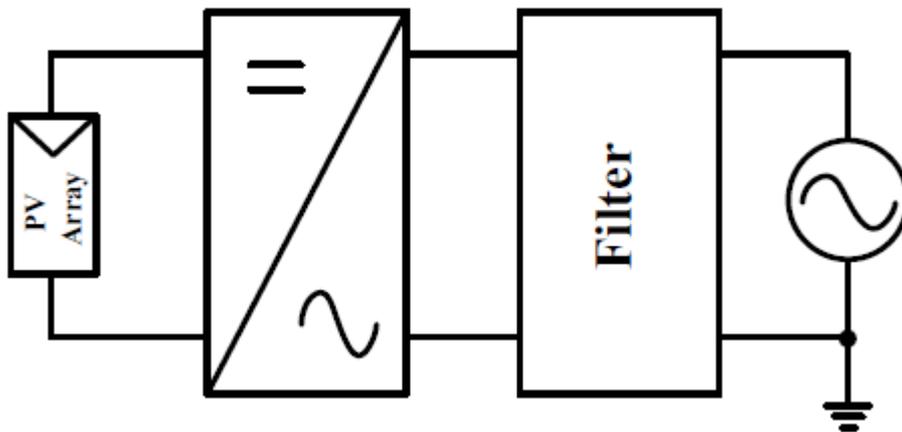


Figure 1.4: Grid connected PV system with transformerless inverter

However, there is a drawback of the absence of the transformer which is DC current leakage into the AC output, that leads to the overloading of the magnetic elements in distribution transformers, and overheating and the other possible failures [4].

As presented in [5], a comprehensive study was done by the PV industry magazine with using a database of more than 400 commercially available PV systems. The maximum efficiency of these systems is illustrated in Figure 1.5, where circles (o) represent transformerless inverters, asterisks (*) represent low-frequency transformer inverters with galvanic isolation between the grid and PV, and triangles (Δ) represent high-frequency DC-DC topologies.

The result of the data shows that, for PV systems up to 6.5 kW, inverters with galvanic isolation achieve maximum efficiencies ranging from 96% to 96.5%, while transformerless inverters can reach efficiencies as high as 98%.

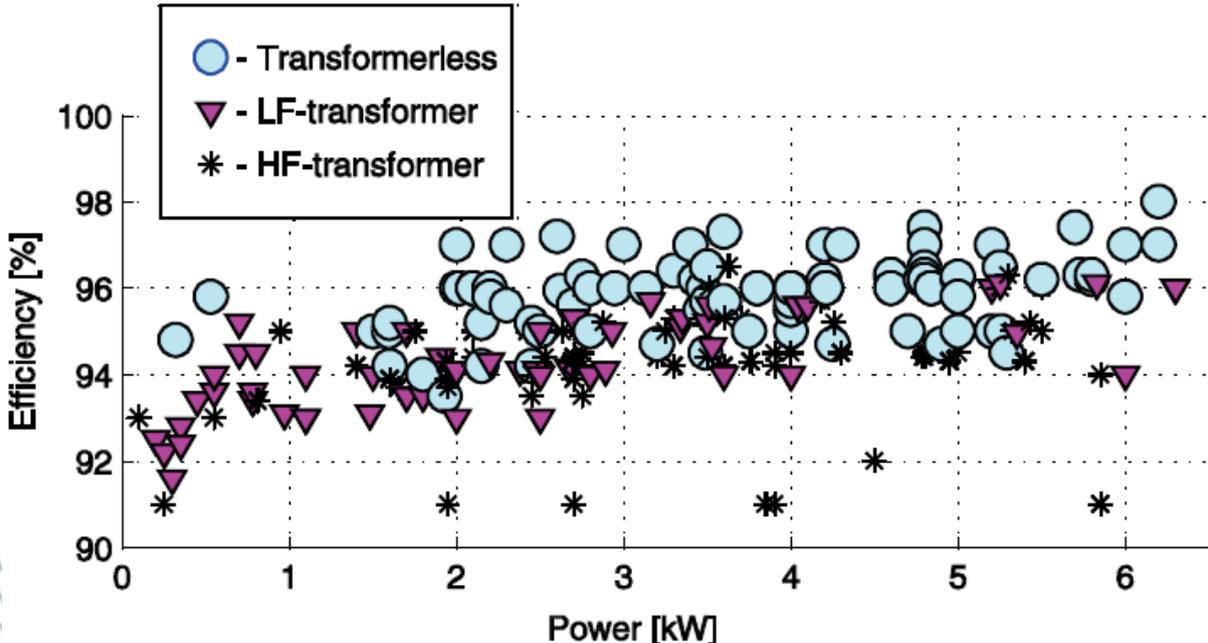


Figure 1.5: PV Inverter Comparison, based on Photon database

1.3 Grid requirements

A photovoltaic system connected to the grid should follow standards that is established by local utilities in line with national regulations. These standards generally include the following aspects [6]:

- Total Harmonic Distortion (THD) and individual harmonic current levels
- Power factor (PF)
- Level of injected DC current
- Voltage and frequency range for normal operation
- Detection of islanding operation (islanding or non-islanding functions)
- Automatic reconnection and synchronizing
- Grounding of the system

A summary of several international grid codes and standards relating to these parameters is presented in Table 1.1 [7].

Table 1.1: Grid codes and grid-connected PV system standards

Standard Name and Origin	(THD Limit; Grid Frequency Limit in Hz; Power Factor Limit; DC Current Injection Limit)
IEEE 1547, USA (IEEE)	(<5%; 57 to 60.5; 0.9–0.97; <0.5% of rated value of output current)
IEEE 929-2000, USA (IEEE)	(<5%; 59.3 to 60.5;>0.85; <0.5% of rated value of output current)
IEC 61727, Swiss (IEC)	(<5%; 49 to 51;>0.90; <1% of rated value of output current)
AS4777, Australia	(<5%; 48 to 52; 0.8–0.95; <0.5% of rated output current/phase)
EN 61000-3-2, England	(<5%; 47.5 to 50.2; NA; <0.22 A corresponding to a 50 W half wave rectifier)
EREC G83, England	(<5%; 49 to 51; 0.95; 0.25% of AC current rating/phase)
VDE 4105, Germany	(<5%; 47.5 to 51.5; 0.89–0.95; <1 A; maximum trip time 0.2 s)
BDEW, Germany	(<5%; 47.5 to 51.5(±5% to +3%); 0.95; NA)
GB/T 19964-2012, China	(<5%; 48 to 50.5; 0.95; <1% of rated output current)
JEAC 9701-2012, Japan	(<5%; 47.5 to 51.5 (Eastern Japan)/57 to 61.8 (Western Japan); 0.9-0.95; NA)

The standards impose a THD limit below 5%, they differ in power factor and DC current injection requirements, the DC current injection is further addressed in Section 1.4. The DC injection limits are either 0.25% of the rated current or 0.22 A, equivalent

to a 50 W half-wave rectifier. Power factor thresholds vary but generally must remain above 0.8 to ensure compliance with minimum performance standards.

An investigation in [4] compares IEC 61727, IEEE 1547, and EN 61000-3-2 standards regarding THD, power factor, and DC current injection, as shown in the Table 1.2. Among these, VDE 0126-1-1 uniquely requires disconnection within 0.2 s if DC injection exceeds 1 A, and it's the only standard that addresses transformerless PV systems. It mandates inverter shutdown if leakage current ≥ 100 mA lasts more than 0.04 s, as also shown in Table 1.3 [7].

Table 1.2: Limit of the injected DC current, for different standards

	IEC61727	VDE0126-1-1	IEEE1547	EN61000-3-2	IEEE 929-2000
DC current injection	< 1 % of rated output current	< 1 A	< 0.5 % of rated output current	< 0.22 A corresponds to a 50 W half-wave rectifier	< 0.5 % of rated output current

Table 1.3: Leakage current values and their corresponding disconnection times listed in the VDE 0126-1-1 standards

Leakage Current Value (mA)	Disconnection Time (s)
30	0.3
60	0.15
100	0.04

1.4 DC current injection

Transformerless grid-connected photovoltaic (PV) inverters, due to the absence of galvanic isolation between the PV array and the utility grid, face a risk of injecting direct current (DC) into the grid. This undesired DC component can result from several factors, including switching asymmetries, sensor offset errors, imperfections in digital control systems, and the non-ideal behavior of semiconductor devices. Although the DC current injected by a single inverter may be very small, the overall effect of multiple inverters operating on the same grid node can lead to serious issues such as distribution transformer saturation, increased power losses, generation of even-order harmonics, and reduced lifespan of grid-connected equipment. To mitigate these risks, international standards such as IEEE 1547 limit the allowable DC injection to no more than 0.5% of the inverter's rated output current [4].

Therefore, minimizing DC injection in transformerless systems requires accurate current sensing, well-calibrated control algorithms, and careful inverter topology design.

1.5 Parasitic capacitance

The AC leakage current is the major problem of the transformerless inverter when are connected to the PV and the grid, as shown in Figure 1.6 (b). This current is caused by a fictitious capacitance that is between the ground and body of the PV array, as shown in Figure 1.6 (a).

Also, this fictitious capacitance is called parasitic capacitance, which is undesirable practically. The parasitic capacitance between the PV frame and earth in large undergrounded PV arrays is typically 50-150 nF/kW [7]. This value is not constant and the rating of this parasitic capacitance depends on some important factors, which are Structure of solar panel and frame, Surface of solar cell, Distance between solar cells, Weather condition Humidity, Dust or salt covering the PV panels and etc.

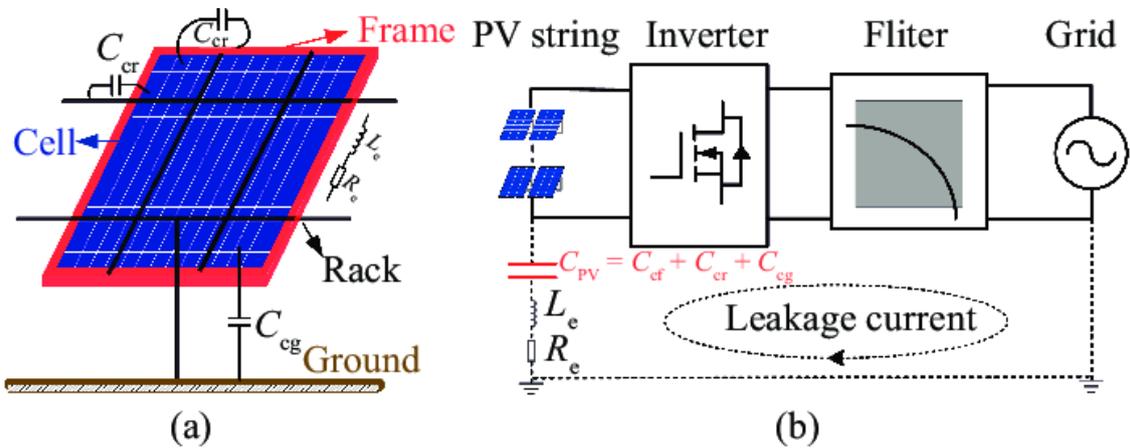


Figure 1.6: parasitic capacitance (a), leakage current (b)

1.6 Common-mode voltage in single-phase systems

Figure 1.7 shows a part of the single-phase grid-connected PV system with a transformerless inverter. The output voltages V_{AN} and V_{BN} , generated by the inverter legs, are pulsed waveforms and these voltage pulses drive leakage current through the parasitic capacitance C_{PV} between the PV array and ground, as illustrated in Figure 1.8.

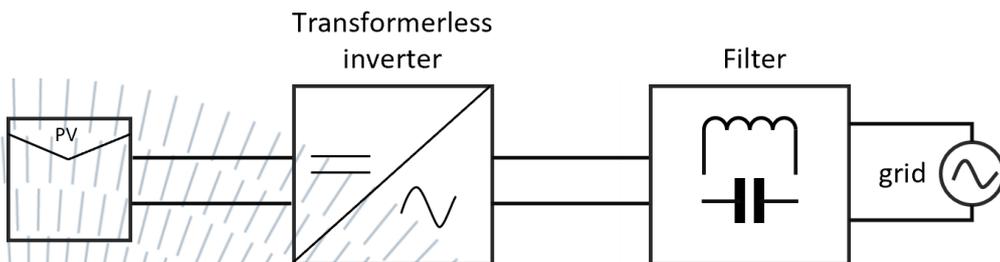


Figure 1.7: Single-phase grid-connected PV systems with transformerless inverter

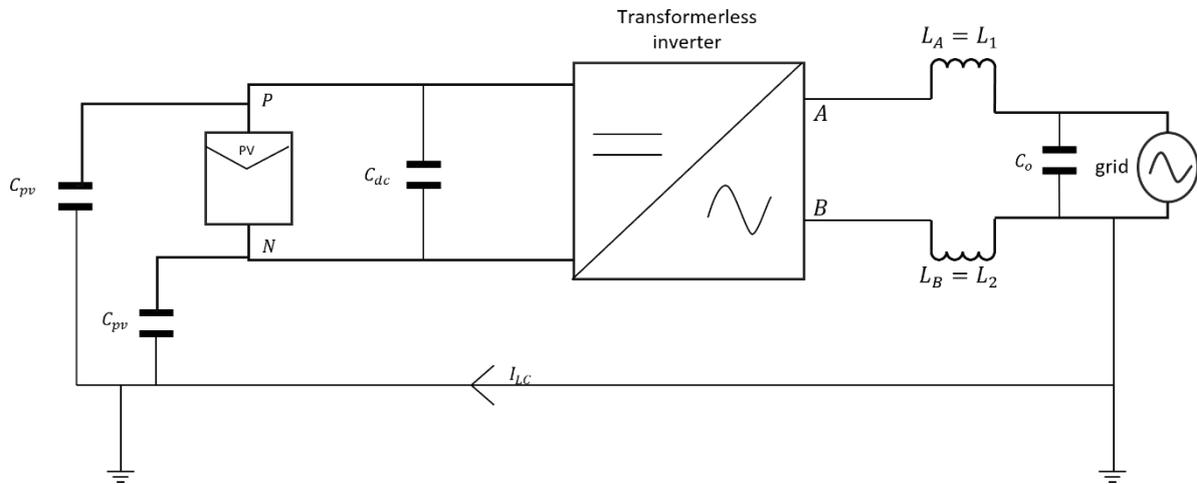


Figure 1.8: Primary common mode model of single-phase grid-connected PV with transformerless

In transformerless PV inverter systems, the negative terminal “N” of the photovoltaic (PV) modules is typically used as the reference point. The midpoints “A” and “B” of the inverter bridge legs operate as the AC output terminals. The voltage across the PV array, denoted as V_{PN} , represents the differential voltage between the positive terminal “P” and the negative terminal “N”. The common-mode voltage (CMV) and differential-mode voltage (DMV) are defined based on the voltages from nodes A and B to reference point N, represented as V_{AN} and V_{BN} , respectively.

While the effect of the output filter inductance remains significant, the effects of the filter capacitor and the grid impedance can often be neglected in high-frequency leakage current modeling [7, 8]. As a result, the final common-mode equivalent circuit is shown in Figure 1.9, where the total common-mode voltage V_{tCM} acts as a source of the leakage current I_{LC} .

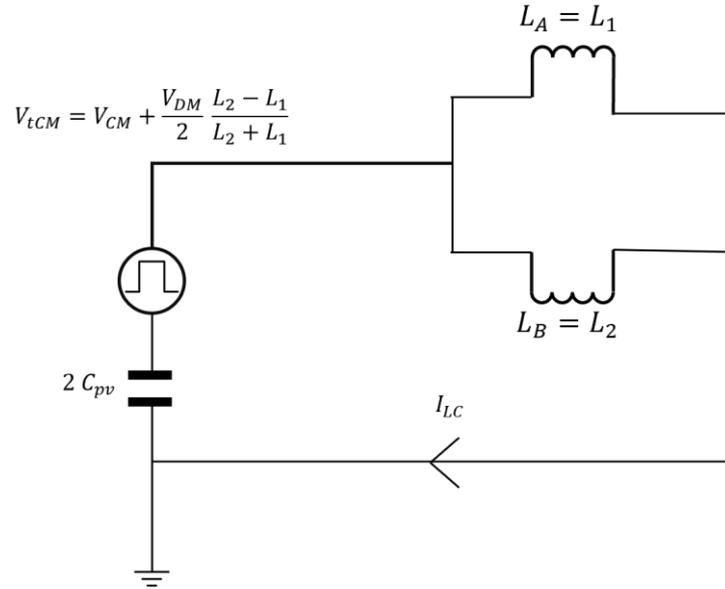


Figure 1.9: Final common mode model of single-phase grid-connected PV with transformerless inverter

The common mode voltage (V_{CM}) and differential mode voltage (V_{DM}) can be defined as demonstrated in Equations (1.1) and (1.2) [7].

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} \quad (1.1)$$

$$V_{DM} = V_{AN} - V_{BN} \quad (1.2)$$

V_{AN} and V_{BN} are respectively defined based on V_{CM} and V_{DM} :

$$V_{AN} = V_{CM} + \frac{V_{DM}}{2} \quad (1.3)$$

$$V_{BN} = V_{CM} - \frac{V_{DM}}{2} \quad (1.4)$$

From Equations (1.3) and (1.4), it is clear that the voltages at terminals A (V_{AN}) and B (V_{BN}) are composed of both common-mode and differential-mode components. These

voltages are the primary source of the leakage current. The effect of the filter inductors is significant, while the effects of the grid and the filter capacitors can be neglected [7]. Therefore, an accurate estimation of the leakage current requires identifying the voltage that drives it which is known as the total common-mode voltage V_{tCM} .

Due to the inductive imbalance in the output branch, V_{tCM} can be calculated by using a weighted average of the branch voltage [9].

$$V_{tCM} = \frac{L_B V_{AN} + L_A V_{BN}}{L_A + L_B} \quad (1.5)$$

By substituting Equations (1.3) and (1.4) into Equation (1.5).

$$V_{tCM} = \frac{L_B(V_{CM} + \frac{V_{DM}}{2}) + L_A(V_{CM} - \frac{V_{DM}}{2})}{L_A + L_B} \quad (1.6)$$

$$V_{tCM} = \frac{(L_B + L_A)V_{CM} + \frac{V_{DM}}{2}(L_B - L_A)}{L_A + L_B} \quad (1.7)$$

$$V_{tCM} = V_{CM} + \frac{V_{DM}}{2} \frac{L_B - L_A}{L_B + L_A} \quad (1.8)$$

Equation (1.8) demonstrates that the total common mode voltage dependent on both the conventional common mode component V_{CM} and differential voltage V_{DM} weighted by the inductance imbalance.

In the special case, when $L_A = L_B$ Equation 1.8 can be simplified as:

$$V_{tCM} = V_{CM} = \frac{V_{AN} + V_{BN}}{2} \quad (1.9)$$

It is desirable that the CM voltage of the inverters be kept constant in all operating modes. As a result, it features excellent leakage currents characteristic. However, in

some designs of full-bridge transformer less inverters, the CM voltage are not kept constant in all operating modes, which leads to high leakage currents.

Amplitude and spectrum of leakage current depends on the converter topology, on the switching strategy and on the resonant circuit formed by the parasitic capacitance to the ground, the converter, the AC filter and the grid.

1.7 Leakage ground current

The leakage current causes electrical risks when a person touches the PV array. This current can flow through the human body to the ground, and it can lead to a shock or resulting in personal injury. Also, if the leakage current is above a certain level, it can lead to PV array damage. Furthermore, the leakage current increases the EMI. Thus, this current can cause failure in the power conditioning systems (PCS) and these electronic devices.

The voltage fluctuation V_{PV} across C_{PV} is caused by the high-frequency switching. At this time, the leakage current I_{LC} is occurred by V_{PV} and flows between the PV array and the grid as shown in Figure 1.6 (b).

Advanced inverter topologies like HERIC and H5 mitigate this issue by implementing decoupling methods during freewheeling states. in contrast to conventional H-bridge inverters, that permit common-mode voltage fluctuations, HERIC on the AC side and H5 on the DC side effectively reducing leakage current.

1.8 Pulse Width Modulation techniques

1.8.1 Bipolar PWM

Figure 1.10 shows a full bridge inverter that includes four switches. In this PWM technique, switches (T1, T4) [TA+, TB-] and (T2, T3) [TA-, TB+] are switches pairs meaning that they are ON or OFF simultaneously. So, in the ideal situation one of these two pairs is on and the other one is OFF.

The switching signal is generated by comparing the carrier signal (v_{tri}) with the control signal ($v_{control}$). Switches T1 and T4 are ON when $v_{control} > v_{tri}$. While switches T2 and T3 are ON when $v_{control} < v_{tri}$ as shown in Figure 1.11 [10].

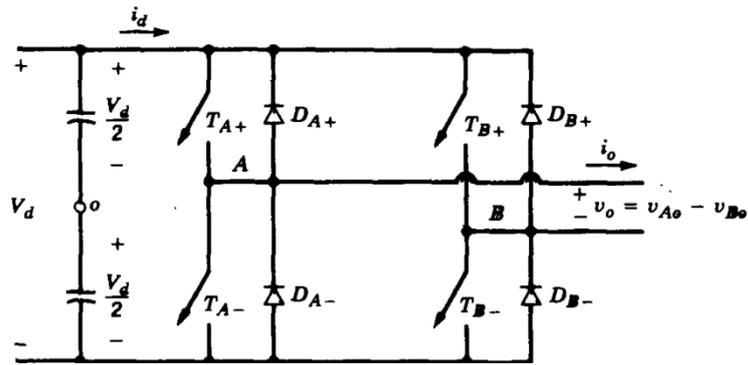


Figure 1.10: Full bridge inverter

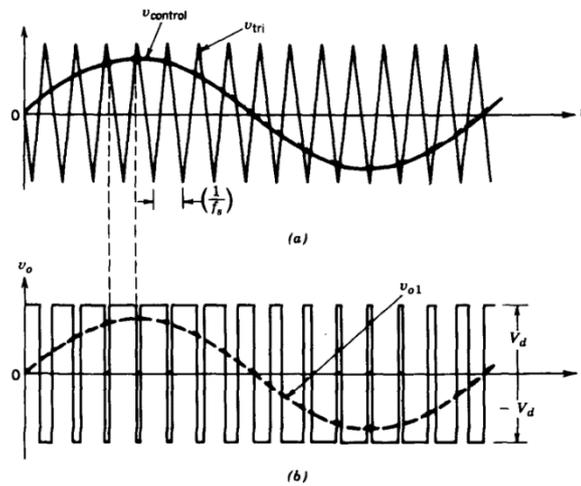


Figure 1.11: Bipolar PWM switching signal

1.8.2 Unipolar PWM

In contrast with bipolar, unipolar PWM switching signal is generating the carrier signal with both the $v_{control}$ and $-v_{control}$. Switches T1(A+) is on if $v_{control} > v_{tri}$, otherwise T2(A-) is ON. Similarly, Switches T3 (B+) is ON if $v_{control} > v_{tri}$, otherwise T4(B-) is ON as shown in Figure 1.12 [10].

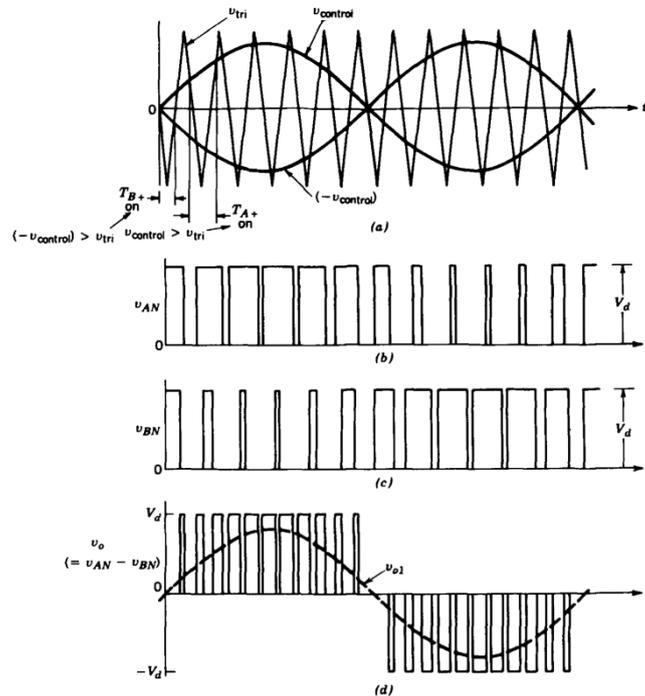


Figure 1.12: Unipolar PWM switching signal

From Figure 1.12 it can be concluded that, when the ON switches are:

1. T1 and T4 (TA+ and TB-), $v_{AN} = V_d, v_{BN} = 0; v_o = V_d$
1. T2 and T3 (TA- and TB+), $v_{AN} = 0, v_{BN} = V_d; v_o = -V_d$
2. T1 and T3 (TA+ and TB+), $v_{AN} = V_d, v_{BN} = V_d; v_o = 0$
3. T2 and T4 (TA- and TB-), $v_{AN} = 0, v_{BN} = 0; v_o = 0$

Therefore, this technique results in three output voltage levels ($+V_{DC}, 0$ and $-V_{DC}$). The main advantage of this technique is that the switching frequency effectively doubling. This is an advantage as the lowest harmonics of the output voltage appears in the twice of the switching frequency resulting significant reduction in the harmonic content. In addition, the voltage jump reduced from $2V_d$ (as in the bipolar PWM) to V_d in this technique.

2. Design and Control of Inverter Components

In this chapter, the key component of the inverter is analyzed to achieve the requirements of the inverter. The components analyzed are the power semiconductor switches, the dc-link and the output filter.

2.1 Power Semi-conductor Switches

One of the main components of the inverter is the power switches. The main goal of the switch is to convert the PV system DC voltage to AC voltage. Hence, it must tolerate the DC-link voltage, output current and the switching frequency while minimizing the losses.

2.1.1 Switches Basics

In contrast to diodes and thyristors, controllable switches (like IGBTs and MOSFETs) both turned on and off by a controlled signal allowing a high-quality conversion. The diagram of a general ideal controllable switch is shown in Figure 2.1 [10].

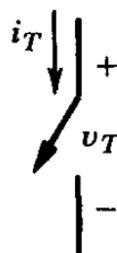


Figure 2.1: Controllable switch

When the switch is off, no current passes. When it is on, the current can only circulate in the direction of the arrow.

2.1.2 Ideal Switches

The characteristics of the ideal switches [10]:

1. When off, no current flow while clocking large forward and reverse voltage
2. When on, the current circulates with zero voltage drop
3. Instantaneously switched from off to on and vice versa
4. Negligible power is required to control the switch

However, the available switches are non-ideal. Therefore, they will dissipate power. To prevent the failure of the switch, the dissipated power must be minimized.

2.1.3 Actual Switches losses analysis

To analyze the power dissipation, a simple circuit of a controllable switch is presented in Figure 2.2(a), where the diode is assumed ideal to focus on the switch. As shown in Figure 2.2(b) when the switch is on, the current I_o circulates through the switch while the diode is reverse biased. On the other hand, when the switch is off, the current I_o flows through the diode where the voltage appears across the switch is V_d .

Figure 2.2(b) shows the transition during the turning on of the switch. Starting with delay time $t_{d(on)}$ which can be neglected. Then, there is the current rise time t_{ri} where the current rise from 0 to I_o . When the switch current value reach to I_o , the diode becomes reversed biased. Followed by the voltage fall time t_{fv} where the voltage falls from V_d to V_{on} . It can be concluded that the switch is subjected to higher values of both voltage and current simultaneously during the turn-on crossover interval $t_{c(on)}$. Given that [10]:

$$t_{c(on)} = t_{ri} + t_{fv} \quad (2.1)$$

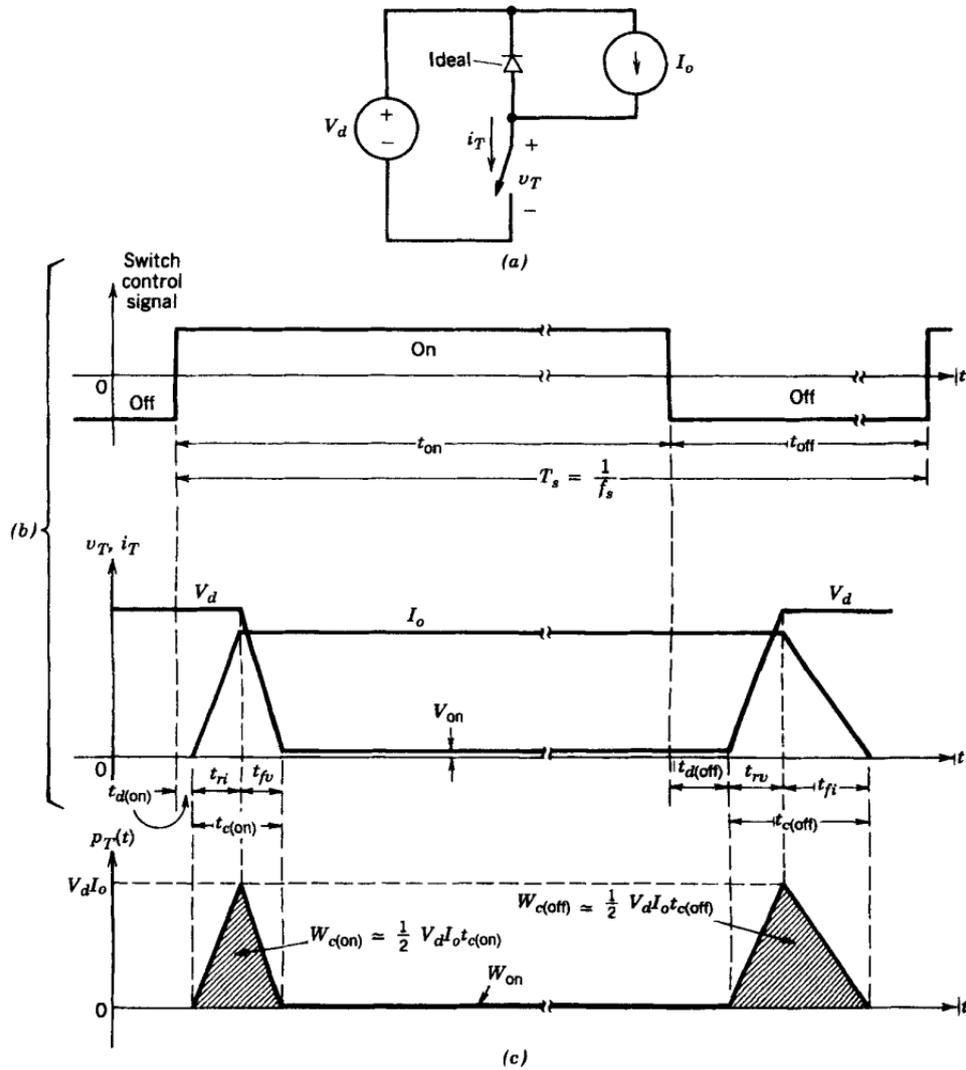


Figure 2.2: Characteristics of actual power switch

Figure 2.2(c) presents the instantaneous switching power losses. Therefore, the dissipated energy $W_{c(on)}$ during the turn-on transition is calculated by integrating the power losses across the $t_{c(on)}$ as presented in Equation (2.2) [7].

$$\begin{aligned}
 W_{c(on)} &= \int_0^{t_{c(on)}} p_T(t) dt \\
 &= \frac{1}{2} V_d I_o t_{c(on)}
 \end{aligned}
 \tag{2.2}$$

Similarly, the transition during the switching off starts with delay time $t_{d(off)}$. Thereafter, voltage rise time t_{rv} where voltage increases from V_{on} to V_d . Followed by the current fall time t_{fi} , the switch current starts to reduce from I_o to 0. In conclusion the switch is subjected to higher values of both voltage and current simultaneously during the turn-off crossover interval $t_{c(off)}$. Given that:

$$t_{c(off)} = t_{rv} + t_{fi} \quad (2.3)$$

Where the energy dissipated during the turn off transition is given by:

$$W_{c(on)} = \frac{1}{2} V_d I_o t_{c(off)} \quad (2.4)$$

From the previous Equations, the average switching power losses:

$$\begin{aligned} P_S &= \frac{\frac{1}{2} V_d I_o t_{c(on)} + \frac{1}{2} V_d I_o t_{c(off)}}{T_s} \\ &= \frac{1}{2} V_d I_o f_s (t_{c(on)} + t_{c(off)}) \end{aligned} \quad (2.5)$$

From Equation (2.5), important conclusions can be determined. The average switching losses directly proportional to the switching frequency and the switching times. Therefore, switches with shorter switching times are desirable.

After analyzing the switching period, it is worth analyzing the conduction period. When the switch is fully on, the switch voltage decreases but does not vanish, however reaches to low value of V_{on} . In addition, the current I_o flow through the switch during the conduction time t_{on} .

From Figure 2.2 the dissipated energy during the conduction period can be represented by:

$$W_{on} = V_{on}I_o t_{on} \quad (2.6)$$

Consequently, the average power dissipation during the conduction state (P_{on}) is given by:

$$P_{on} = V_{on}I_o \frac{t_{on}}{T_s} \quad (2.7)$$

From Equation (2.7), it shows that for lower conduction losses, V_{on} should be reduced. Finally, when the switch is off, the leakage current is approximately zero and could be neglected. Therefore, the average power losses in the switch are the sum of the switching and conduction losses.

$$P_{Total}^T = P_s + P_{on} \quad (2.8)$$

In conclusion, the power switch requires some characteristics to ensure reliable operation. In the off state, the switch must restrict the current. In addition, short $t_{c(on)}$ and $t_{c(off)}$ is required to allow the usage of high switching frequencies. Low V_{on} is preferred to reduce the conduction losses. Simultaneously, tolerance of high voltage and high current is essential for the reliable operation. Figure 2.2 illustrate that during switching on and off, both voltage and current are high. Moreover, characteristics such as high di/dt and dv/dt tolerance, low gate power simplify the circuit design and improve the inverter performance.

2.1.4 MOSFET and IGBT

The choice of the switch in the inverter has a significant influence on the switching losses, conduction losses, efficiency and the inverter overall performance. Two commonly used switching devices in modern inverter topologies are MOSFETs and IGBTs.

MOSFETs are voltage-controlled devices with high input impedance and minimum gate drive current requirements. They are characterized by very fast switching speeds, with short $t_{c(on)}$ and $t_{c(off)}$ times in the nanosecond range. This characteristic leads to lower switching losses. The fast-switching speed of MOSFETs make them suitable for high-frequency applications (in range of 30–100 kHz) [10].

MOSFETs are ideal for low-voltage applications, mainly because of their low on-state resistance $r_{DS(on)}$, which reduces conduction losses. However, the efficiency of the MOSFETs in high-voltage applications is limited since the resistance tends to increase dramatically with the increase of the voltage ratings.

IGBTs integrate the high input impedance and voltage-controlled gate of a MOSFET with the high current-carrying capacity and minimal V_{on} . They are better suited for medium- to high-voltage applications, handling voltages in range of 600 V up to several kV. Although IGBTs having slower switching speed than MOSFETs with $t_{c(on)}$ and $t_{c(off)}$ times of 1 μ s, they provide lower V_{on} (in range of 2–3 V in a 1000 V device) that reduces the conduction losses.

In conclusion, MOSFETs are preferable for low-voltage (usually below 500 V) and high-frequency applications (over 30 kHz), because of their quick switching speed and low conduction losses. IGBTs, on the other hand, are better suited for medium-to-high voltage applications (600 V to several kilovolts) that operate at lower switching frequencies (usually below 20 kHz) due to their reduced V_{on} and higher current capabilities.

When it comes to power handling, MOSFETs are more effective and thermally stable in lower-power systems where quick switching is crucial, whereas IGBTs are typically preferred in high-power applications because of their capacity to handle higher currents and tolerate higher voltages.

2.2 Filter design

For grid-connected inverters, filtering is crucial to ensure power quality, grid code compliance and inverter and grid protection. The LCL filter is preferred choice for single-phase inverters due to its superior high-frequency attenuation compared to L or LC filters. This section presents a simplified approach for LCL filters design.

2.2.1 Purpose of LCL filters

The main function of the LCL filter is to reduce the high-frequencies harmonics produced by the inverter's PWM. Hence, the injected power into the grid maintains high quality. Filter size, current ripples, and switching ripples attenuation are the main LCL characteristics to be considered.

2.2.2 LCL Filter Topology

Figure 2.3 illustrates a typical single phase LCL filter. The LCL filter consists of inverter side inductor L_1 , grid side inductor L_2 , and a shunt capacitor C between L_1 and L_2 . Figure 2.3(b) shows the filter with a damping resistor R_D added in series with the capacitor [11].

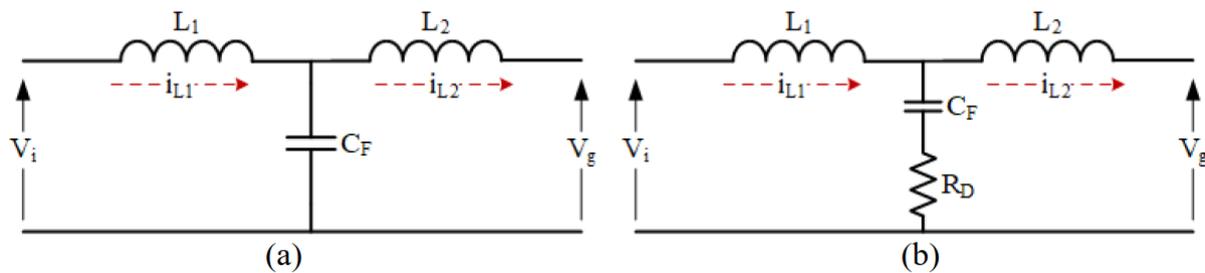


Figure 2.3: Single phase LCL filter (a) without damping (b) with a damping resistor

2.2.3 Filter design procedure

The maximum current ripples ΔI_{Lmax} at the inverter output is given by [12]:

$$\Delta I_{Lmax} = \frac{2V_{DC}}{3L_1} (1 - m) m T_s \quad (2.9)$$

Where m is the modulation index of the inverter. It can be concluded that the peak of the current occurs at $m = 0.5$. Hence the maximum ripples are given by:

$$\Delta I_{Lmax} = \frac{V_{DC}}{6 f_s L1} \quad (2.10)$$

Consequently, the inverter side inductor is given by:

$$L1 = \frac{V_{DC}}{6 f_s \Delta I_{Lmax}} \quad (2.11)$$

Assuming that the ripples limit is 10% of the maximum current as represented in Equation (2.11).

$$\Delta I_{Lmax} = 0.1 I_{max} \quad (2.12)$$

The LCL filter is required to limit the current harmonics to 20%. Therefore, the ripple value is 2% of the current.

The grid side inductor can be designed as a function of $L1$ is presented in Equation (2.13).

$$L2 = rL1 \quad (2.13)$$

Plotting different values of r useful for indicating the transfer function of the filter at a specific resonant frequency.

The size of the filter capacitor C_f has directly impact on the exchanged reactive power with the grid. The reactive power injected by the capacitor is limited to aligning with grid codes, which generally demand that the power factor stay above 0.95.

This constraint is implemented by limiting the filter capacitance C_f to a fraction x of the system's base capacitance C_b , which is calculated based on the base impedance Z_b and grid frequency ω_b as shown in Equation (2.14) [12].

$$\begin{aligned} Z_b &= \frac{V_{ll_{rms}}}{P_n} \\ C_b &= \frac{1}{\omega_b Z_b} \\ C_f &= x C_b \end{aligned} \tag{2.14}$$

Given that $V_{ll_{rms}}$ is the RMS line to line voltage, P_n rated active power, ω_b is the grid frequency.

The capacitor sizing factor x is selected 0.05 to ensure that the reactive power contribution from C_f remains within acceptable limits.

A damping resistor R_f is added in series with the filter capacitor C_f to reduce the resonance effects inherent in LCL filters. The main function of R_f is to attenuate the gain spike that occurs at the filter's natural resonant frequency. This improves the system stability and the inverter power quality. The resistor is selected to be one third of the capacitive reactance at the resonant frequency ω_{res} , as given by the expression:

$$R_f = \frac{1}{3 \omega_{res} C_f} \tag{2.15}$$

This empirical rule provides an efficient trade-off between low power loss and effective damping. The resonant frequency is determined by the combined reactive components of the LCL filter as illustrated in Equation (2.16) [12].

$$\omega_{res} = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \tag{2.16}$$

The resonant frequency is restricted with the range in Equation (2.17), to provide sufficient filtering without affecting the grid frequency or the control.

$$10f_g < f_{res} < 0.5 f_{sw} \quad (2.17)$$

In conclusion, LCL filters can effectively attenuate high frequency harmonics in grid connected inverter systems. To achieve effective results, the values of L_1 , L_2 , C_f and R_f must be carefully selected, as detailed and derived in this section.

2.3 Single Phase PV Inverter Control

The control strategy for PV inverter depends on its operation mode. In the grid-tied mode, PV inverter behaves as a current controlled source to produce output reference current. The feedback controller has to ensure the grid synchronization, extracting maximum power from PV panels, injection of active power in a controlled manner and reactive power support.

According to IEEE 1547 and IEC 61727 standards, the total harmonic distortion (THD) of grid current must be below 5%, and the DC injection should not exceed 1% of the rated current. Therefore, the design of an accurate current controller is essential to meet these compliance criteria in transformerless topologies like HERIC and H5 [13].

2.3.1 Control System

The goal of having a controller in the system is to track the reference current, reduce the steady-state error and minimizing the harmonics in the grid current. This ensures the delivery of a good quality sinusoidal output current with minimum harmonics for preventing the distortion.

The control structure consists of two cascaded closed-loop controllers; The inner current loop, responsible for controlling the inverter output current, improves dynamic response and reduces current distortion. The outer voltage loop regulates the DC-link voltage to ensure system stability and optimal power flow [13]. To ensure proper decoupling and fast dynamic performance, the inner current loop operates at a significantly higher bandwidth than the outer voltage loop. The overall control strategy is shown in Figure 2.4 [14].

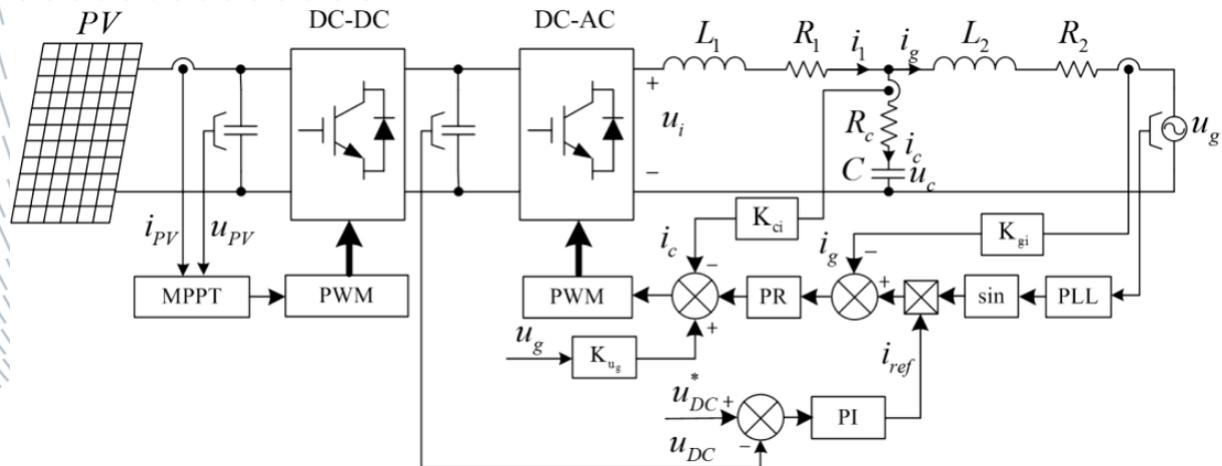


Figure 2.4: Block diagram of the implemented control strategy

2.3.2 Proportional Integral (PI) Controller

PI controllers are the most used and well-established controllers in power electronics because of its simplicity and effectiveness with DC quantities. The transfer function of the PI controller is shown in Equation (2.18). Where K_p and K_i are the proportional and integral gains respectively. The proportional part responds to the instantaneous error, while the integral part eliminates the steady-state error for the DC quantities [13].

$$G_{PI}(s) = K_p + \frac{K_i}{s} = \frac{K_p s + K_i}{s} \quad (2.18)$$

However, the control variables in power electronics applications, the current and voltage, are sinusoidal quantities. Hence, PI controller cannot be directly implemented to regulate the sinusoidal quantities in the stationary reference frame. Hence, PI controllers are typically implemented in the rotating dq reference frame, where AC signals are transformed into DC quantities.

This transformation allows sinusoidal variables to appear as constants, enabling zero steady-state error when using a PI controller. However, the implementation of the dq transformation requires a Phase-Locked Loop (PLL) to track the grid phase angle, which adds complexity, especially in single-phase systems where accurate phase estimation is more challenging.

2.3.3 Proportional Resonant (PR) Controller

The Proportional Resonant (PR) controller is designed to regulate sinusoidal signals efficiently in the stationary frame. The PR provides infinite gain at a certain frequency (resonant frequency) and zero-phase shift. This ensures accurate tracking of sinusoidal reference signals with zero steady-state error. The Laplace-domain transfer function of an ideal PR controller is given by [15]:

$$G_{PR}(s) = K_p + K_i \frac{s}{s^2 + \omega_0^2} \quad (2.19)$$

K_p is the proportional gain term which determines the dynamics of the system such as bandwidth, phase and gain margins. K_i is the resonant (integral) gain term that determines the amplitude gain at a selected frequency and controls the bandwidth around it. ω_0 is the resonant frequency, typically $2\pi 50 \text{ rad/s}$.

Figure (2.5) shows the Bode diagram of an ideal PR controller.

As shown in Figure (2.5), the PR controller exhibits a huge gain centralized at the resonant band. Hence, the PR controller allows following the reference signal with zero state error. Outside this narrow resonant band, the controller gain is nearly unity [14].

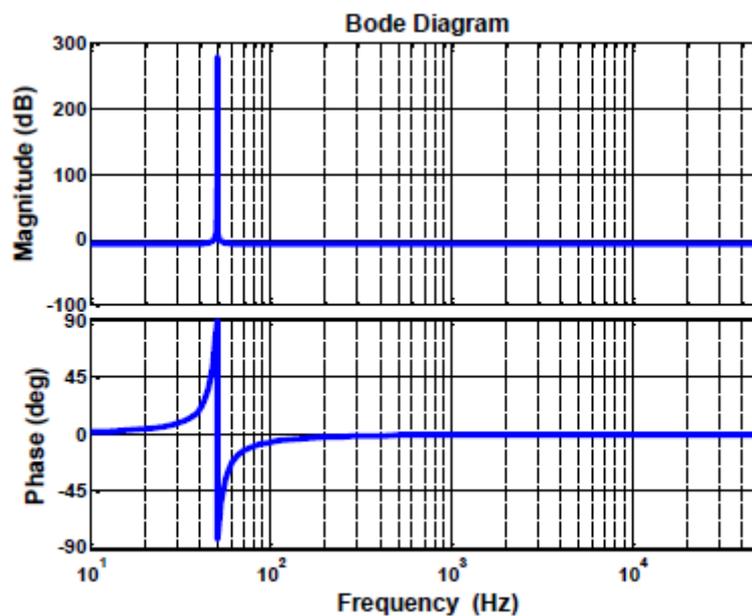


Figure 2.5: Ideal PR controller Bode diagram

2.3.4 Inner Current Loop

The inner current loop is essential for controlling the inverter output current, and ensuring fast dynamic response with disturbance rejection capability. It is the inner most loop of the cascaded control, operating at high bandwidth to track the reference current under varying operating conditions. The block diagram of the current loop is shown in Figure 2.6.

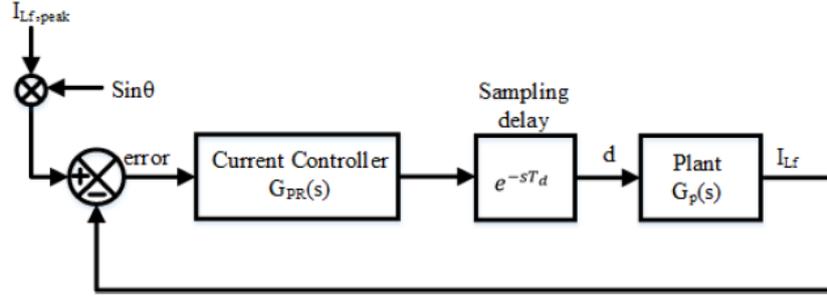


Figure 2.6: Block diagram of the current control loop

Within this loop, The PR controller processes the error between the sinusoidal reference current and the actual output current of the inverter. Thereafter, it generates a control signal (typically a duty cycle input) for switching the inverter's power devices.

In digital implementation, a one-switching-cycle delay is usually considered, because the new control signal is not used until the next switching cycle.

In conclusion, the PR controller acts as part of the inner current control loop and helps the inverter inject an accurate, fast, and distortion-free current into the grid. In the PV systems, a filter is placed between the inverter and the grid to eliminate the switching frequency and ensure injecting current at the grid frequency.

As discussed in the previous section, PR controller aims to provide high gain at the resonant frequency to ensure tracking sinusoidal wave with zero steady state error. However, the ideal PR controller provides infinite gain at the resonant frequency risking the system stability. To address this issue, a non-ideal PR controller with damping part is implemented in [14]. The non-ideal PR controller transfer function is given by:

$$G_{PR}(s) = K_P + \frac{2 K_r \omega_{PRC} s}{s^2 + 2 \omega_{PRC} s + \omega_0^2} \quad (2.20)$$

ω_{PRC} the cutoff frequency that defines the bandwidth around the resonant frequency ω_0 . K_r and K_P are the resonant and proportional gains, respectively. The gain of the controller drops to $\frac{K_r}{\sqrt{2}}$ at both $(\omega_0 - \omega_{PRC})$ and $(\omega_0 + \omega_{PRC})$.

Figure 2.7 shows the Bode diagram of a non-ideal PR controller highlighting the gain behavior around ω_0 .

- Figure 2.7(a) illustrates the bode diagram with fixed K_p at 0.4 and varying K_r .
- Figure 2.7(b) illustrates the bode diagram with varying K_p and fixed K_r at 1.

As shown in Figure 2.7(a), K_r is responsible for the response peak at the target frequency ω_0 . Therefore, it K_r enhances the controller's response allowing it to track the reference value. On the other hand, K_p modifies the overall gain across the frequency range without affecting the peak value at ω_0 . Hence, K_p affects the dynamic response of the controller, while K_r affects peak of the gain around ω_0 [14].

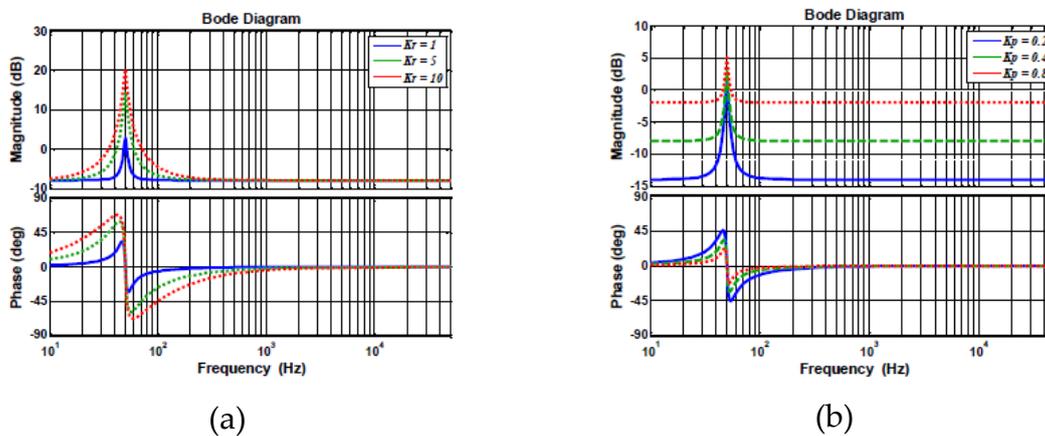


Figure 2.7: Improved PR controller Bode diagram: (a) $K_p = 0.4$; (b) $K_r = 1$.

2.3.5 Outer voltage loop

The outer voltage control loop is implemented to regulate the DC-link voltage under different operation conditions to allow a stable power exchange between the PV system and the grid.

Using a PI controller, the measured and reference voltage are compared to generating the reference current for the inner loop.

As shown in Figure 2.4, this reference current is then tracked by the inner loop to control the inverter output. Moreover, a PLL is used to extract the grid phase which is essential for synchronizing the injected current with the grid [14].

It is worth noting that the voltage PI controller is tuned such that the bandwidth of the inner current loop is significantly higher than the outer voltage loop (in terms of 10 times) to ensure decoupling between the two loops. Consequently, the inner current loop manage has a stable and fast operation while following the reference current generated from the voltage loop.

3. Full Bridge Inverter

3.1 Common-mode voltage in H-Bridge inverter

Figure 3.1 illustrates a single-phase H-bridge inverter equipped with an output filter and a parasitic capacitance C_{PV} between the PV array and ground. This parasitic capacitance provides a path for leakage current to flow through the system, as shown in the simplified model of the H-bridge inverter [16].

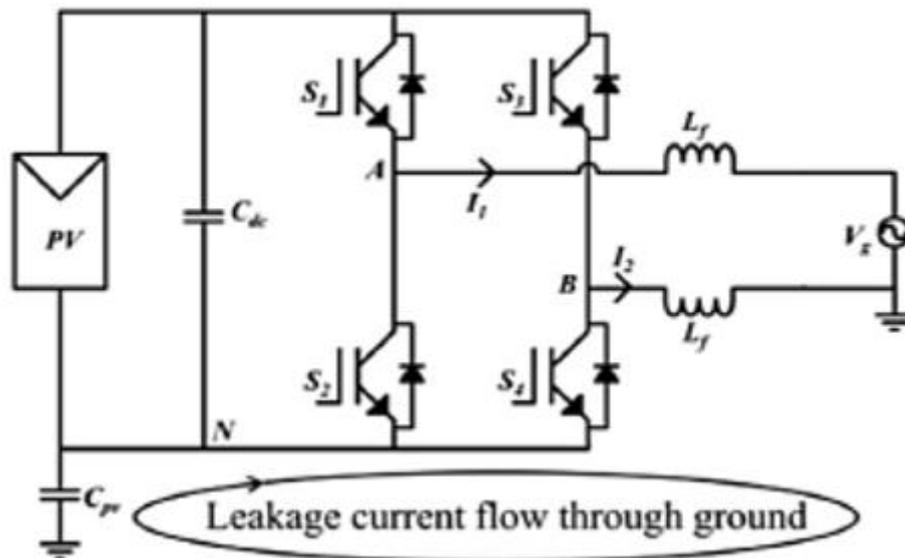


Figure 3.1: H-bridge inverter

Any change in the inverter's common-mode voltage that is explained in Section 1.6 will cause a common-mode current as described by Equation (3.1).

$$i_{CM} = C_{PV} \frac{dV_{CM}}{dt} \quad (3.1)$$

To minimize leakage current in a single-phase H-bridge inverter, it is essential to maintain the constant common-mode voltage (V_{CM}) throughout each switching cycle. When V_{CM} remains constant, its time derivative $\frac{dV_{CM}}{dt}$ becomes zero, thereby preventing the generation of common-mode current in the grounding path [16].

3.2 Performance and Operation of H-Bridge topology with Bipolar PWM

For H-bridge topology, two modulation techniques could be used: unipolar and bipolar modulation. Bipolar PWM is the simplest technique in which switches S1 and S4 are modulated as complementary to switches S2 and S3.

Figure 3.2 illustrates the bipolar H-bridge switching pattern. Noting that all the switches operate at high frequency [17].

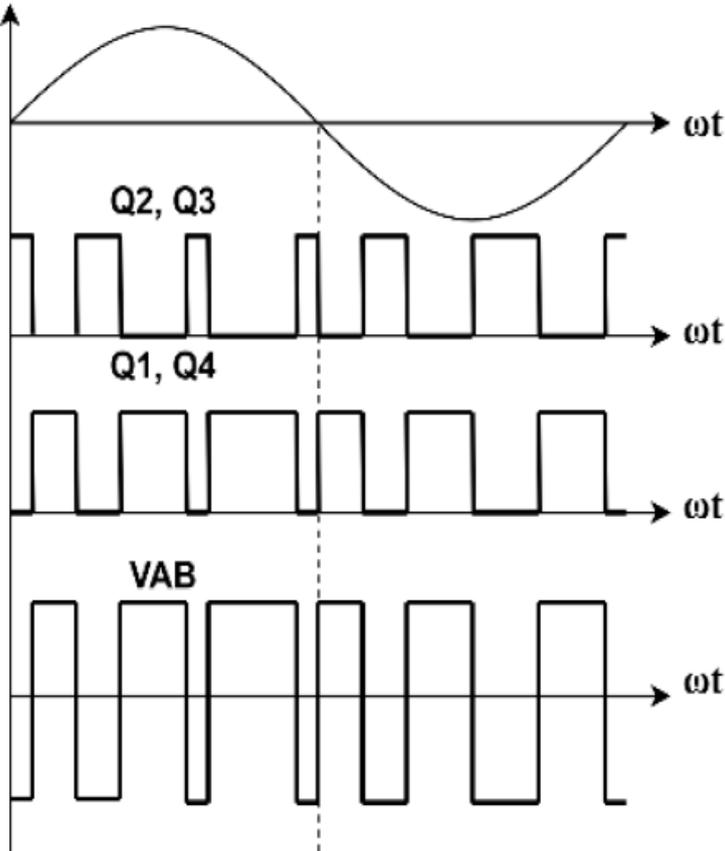


Figure 3.2: Switching pattern in bipolar H-Bridge topology

In bipolar modulation, there are 4 operation modes as shown in Figure 3.3. Mode 1 and 3 represent the power delivery from the PV to the grid, while mode 2 and 4 shows the return of power to the DC-link.

In mode 1, both Switches 1 and 4 operate while switches 2 and 3 are off. From Equations (1.1) and (1.2) the differential and common mode voltage in mode 1:

$$\begin{cases} V_{DM} = V_{in} \\ V_{CM} = \frac{V_{in}}{2} \end{cases} \quad (3.2)$$

In mode 2, the voltages are given by:

$$\begin{cases} V_{DM} = -V_{in} \\ V_{CM} = \frac{V_{in}}{2} \end{cases} \quad (3.3)$$

In mode 3, power is delivered to the grid similar to mode 1. As shown in Figure 3.3(c) both switches 2 and 3 are on where the differential and common mode voltages are given by:

$$\begin{cases} V_{DM} = -V_{in} \\ V_{CM} = \frac{V_{in}}{2} \end{cases} \quad (3.4)$$

Finally, mode 4 is shown in Figure 3.3(d) where:

$$\begin{cases} V_{DM} = V_{in} \\ V_{CM} = \frac{V_{in}}{2} \end{cases} \quad (3.5)$$

The voltage characteristics of H-bridge inverter with unipolar modulation is summarized in Table 3.1.

Table 3.1: Voltage characteristics of the bipolar H-Bridge inverter

Mode	S1	S2	S3	S4	V_{AN}	V_{BN}	V_{DM}	V_{CM}
1	ON	OFF	OFF	ON	V_{in}	0	V_{in}	$\frac{V_{in}}{2}$
2	ON	OFF	OFF	OFF	V_{in}	V_{in}	$-V_{in}$	V_{in}
3	OFF	ON	ON	OFF	0	V_{in}	$-V_{in}$	$\frac{V_{in}}{2}$
4	OFF	ON	OFF	OFF	0	0	V_{in}	$\frac{V_{in}}{2}$

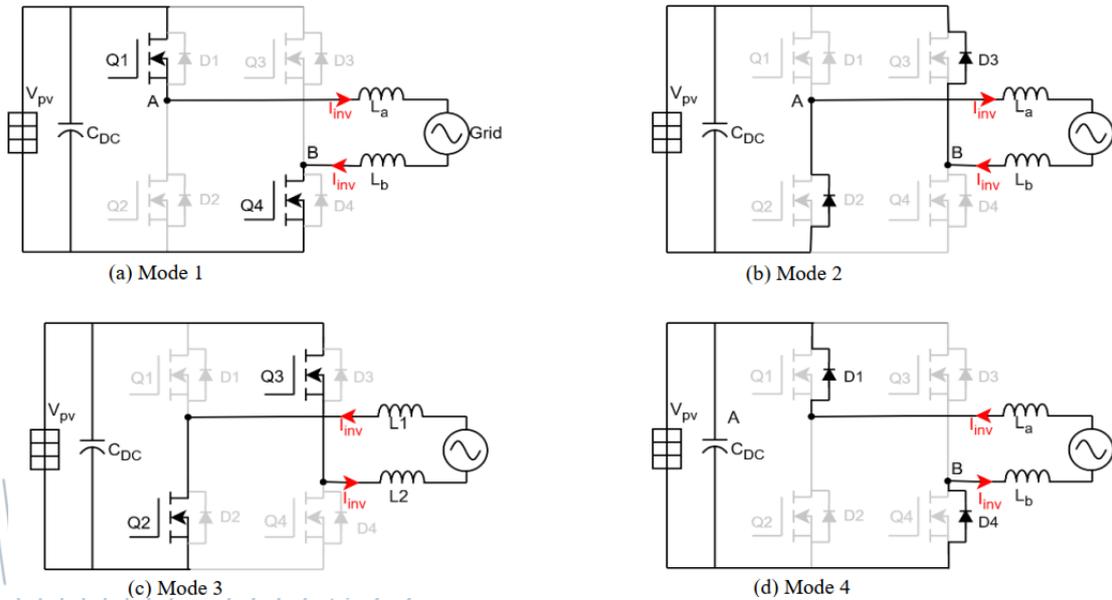


Figure 3.3: Operation modes of H-bridge inverter with Bipolar modulation

From Table 3.1, it shows that bipolar modulation for H-bridge achieves constant V_{CM} . Therefore, low leakage current is ensured as expressed in Equation (3.1). On the other hand, the V_{DM} characteristics are undesirable with only 2 levels (V_{in} and $-V_{in}$). Consequently, the output voltage is characterized by relatively high THD

Although this technique is simple, it has a drawback which is low conversion efficiency. The main cause of this inefficiency is the behavior of the grid current during the freewheeling period; the grid current flows through the body diodes of the inactive switches and returns to the DC-link capacitor. This current path increases the

conduction losses due to the voltage drop across the diodes and switches. Moreover, the repeated circulation of the current through the DC-link introduces additional stress and ripple on the capacitor, contributing to switching and conduction losses. These factors together reduce the overall energy conversion efficiency of the system.

Another key component of this technique is the grid-side filter. In [4], two types of filters were analyzed. The first configuration consists of an inductor placed only in the line branch, while the second includes inductors in both the line and neutral branches, as illustrated in Figure 3.4.



Figure 3.4: LCL filter a) Filter 1 configuration b) Filter 2 configuration

When employing the first filter configuration, the PV voltage to ground shows a high-frequency component with a significant amplitude at the switching frequency (10 kHz) and its harmonics, as shown in Figure 3.5. These voltage changes can cause leakage currents when interacting with parasitic capacitance. This issue occurs due to the time varying voltage across the parasitic capacitor, which results in leakage current as expressed in Equation (3.1). At high frequency, the rate of voltage changes $\frac{dv}{dt}$ increases. Consequently, the leakage current amplifies. As a result, this filter configuration is considered unsuitable for transformerless inverter applications due to the associated safety and efficiency concerns.

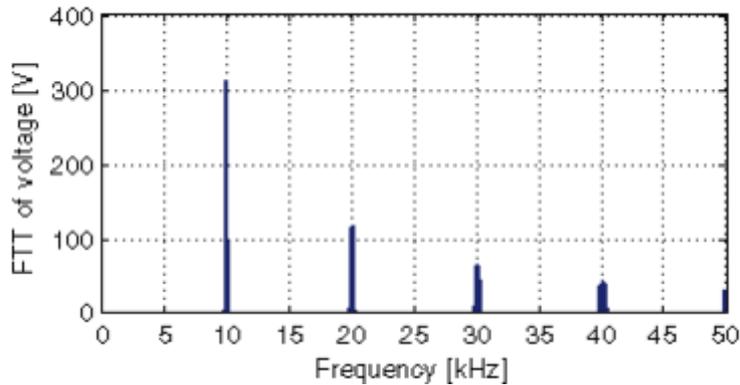


Figure 3.5: The results, voltage to ground with a bipolar PWM (LCL filter 1).

In contrast, the second filter configuration, when combined with a bipolar PWM technique, produces a constant common-mode voltage.

Furthermore, Figure 3.6 demonstrates the voltages between the PV positive and negative terminals to the ground. The PV voltage to ground fluctuates at the grid frequency, with its amplitude limited to half the peak value of the grid voltage. This is because the additional inductor between the inverter and the grounded capacitor increases the impedance for high-frequency components, thereby attenuating voltage fluctuations at the PV-to-ground node. This behavior significantly reduces leakage current and makes this configuration more appropriate for transformerless inverter systems.

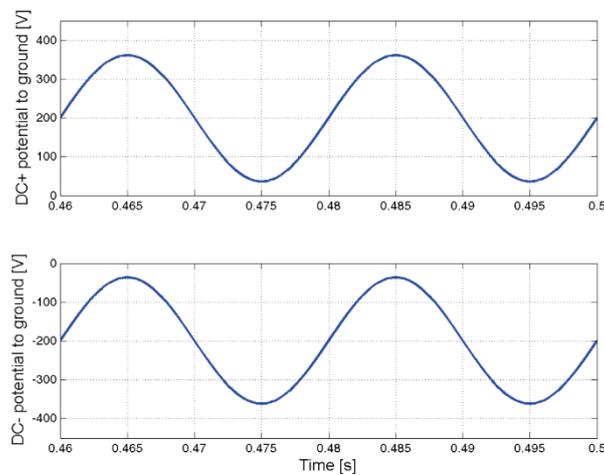


Figure 3.6: The results, voltage to ground with a bipolar PWM (LCL filter 2).

Figure 3.7 present the simulation results of H-Bridge inverter with Bipolar PWM, showing the load current, the voltage between DC negative terminal and the ground, and the leakage current [16]. The simulation confirms a minimal leakage current due to the low $\frac{dv}{dt}$ and purely sinusoidal common-mode voltage as illustrated in Figure 3.7.

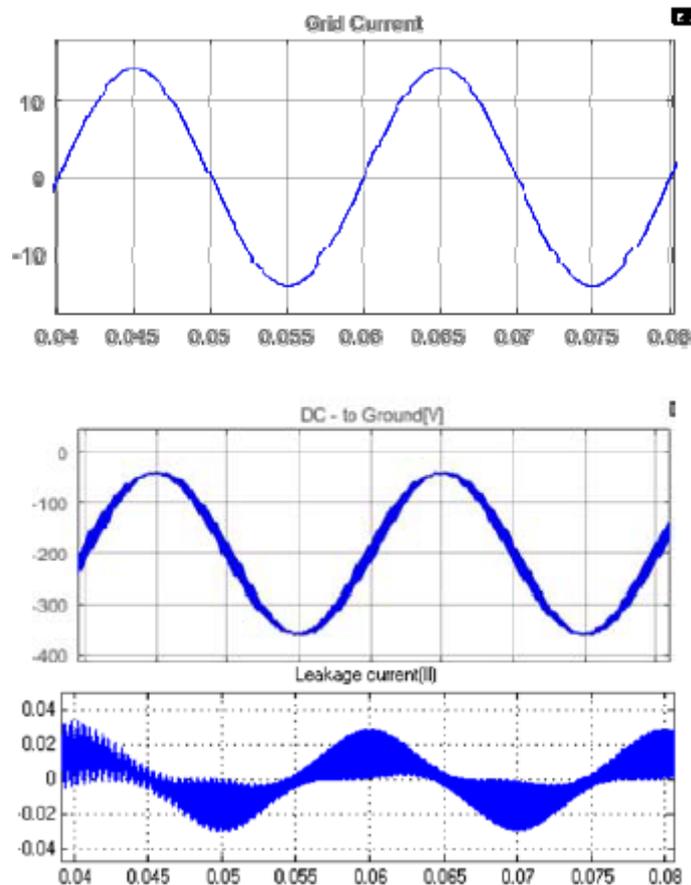


Figure 3.7: H-bridge, BPWM: load current, voltage to ground and ground leakage current

In conclusion, bipolar modulation for H-bridge, having the grid filter where its inductor is distributed equally on the line, solved the issue of the leakage current. Therefore, it is possible to be used for the transformerless systems. However, it is not widely used because of the low conversion efficiency.

3.3 Performance and Operation of H-Bridge topology with Unipolar PWM

For H-bridge topology, two modulation techniques could be used; unipolar and bipolar modulation. Figure 3.8 illustrates the unipolar H-bridge switching pattern. Switches 1 and 2 operate at grid frequency, while switches 3 and 4 operate at high switching frequency [17].

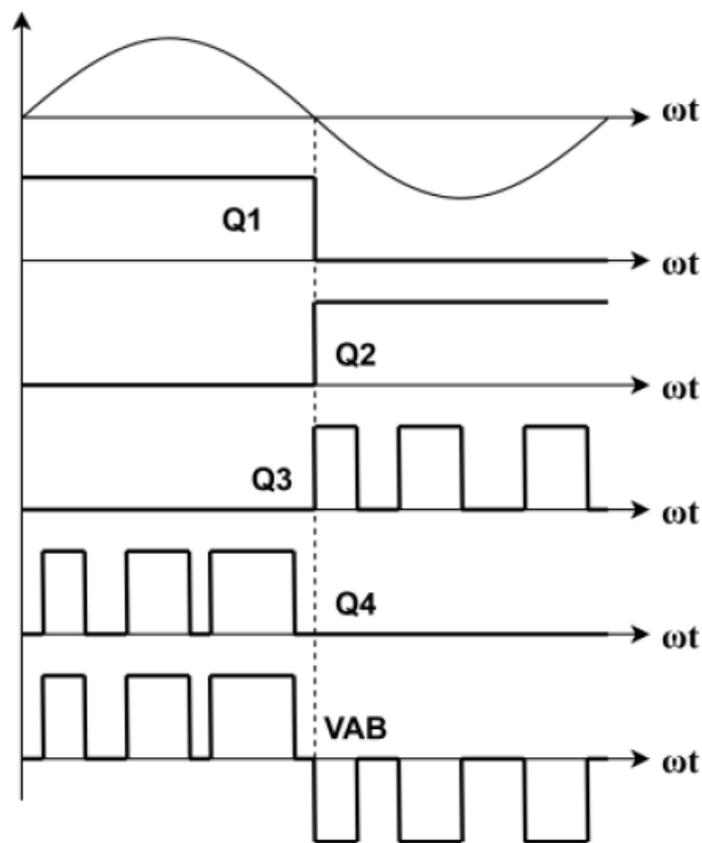


Figure 3.8: Switching pattern in unipolar H-Bridge topology

In unipolar modulation, there are 4 operation modes as shown in Figure 3.9. Mode 1 and 3 represent the power delivery from the PV to the grid, while mode 2 and 4 illustrate the freewheeling stages.

In mode 1, both Switches 1 and 4 operate while switches 2 and 3 are off. From Equations (1.1) and (1.2) the differential and common mode voltage in mode 1:

$$\begin{cases} V_{DM} = V_{in} \\ V_{CM} = \frac{V_{in}}{2} \end{cases} \quad (3.6)$$

In mode 2, only switch 1 is on while other switches are off. Consequently, the voltages are given by:

$$\begin{cases} V_{DM} = 0 \\ V_{CM} = V_{in} \end{cases} \quad (3.7)$$

In mode 3, power is delivered to the grid similar to mode 1. As shown in Figure 3.9(c) both switches 2 and 3 are on where the differential and common mode voltages are given by:

$$\begin{cases} V_{DM} = -V_{in} \\ V_{CM} = \frac{V_{in}}{2} \end{cases} \quad (3.8)$$

Finally, mode 4 is shown in Figure 3.9(d) where:

$$\begin{cases} V_{DM} = 0 \\ V_{CM} = 0 \end{cases} \quad (3.9)$$

The voltage characteristics of H-bridge inverter with unipolar modulation is summarized in Table 3.2.

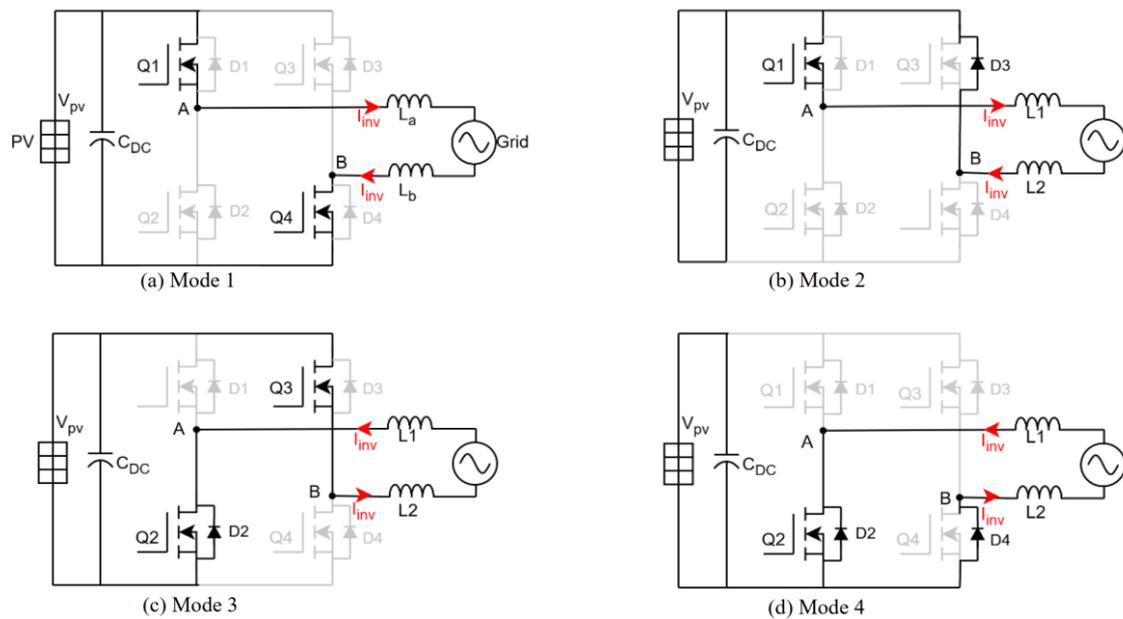


Figure 3.9: Operation states of H-bridge inverter with Unipolar modulation

Table 3.2: Voltage characteristics of the unipolar H-Bridge inverter

Mode	S1	S2	S3	S4	V_{AN}	V_{BN}	V_{DM}	V_{CM}
1	ON	OFF	OFF	ON	V_{in}	0	V_{in}	$\frac{V_{in}}{2}$
2	ON	OFF	OFF	OFF	V_{in}	V_{in}	0	V_{in}
3	OFF	ON	ON	OFF	0	V_{in}	$-V_{in}$	$\frac{V_{in}}{2}$
4	OFF	ON	OFF	OFF	0	0	0	0

From Table 3.2, V_{DM} has 3 different values ($+V_{in}$, 0, and $-V_{in}$) in each cycle. Which is desirable characteristic as it leads to high conversion efficiency and reduces the THD.

However, a major drawback of this modulation strategy is generating a varying common-mode voltage. Where the change in V_{CM} leading to a huge leakage current as expressed in Equation (3.1). Therefore, this modulation strategy with H-Bridge topology is not feasible in the transformer less PV system.

As observed in [16] the UPWM strategy applied to the H-bridge results in significant leakage current due to high-frequency components in the common-mode voltage as shown in Figure 3.10 which is aligned with the theoretical analysis.

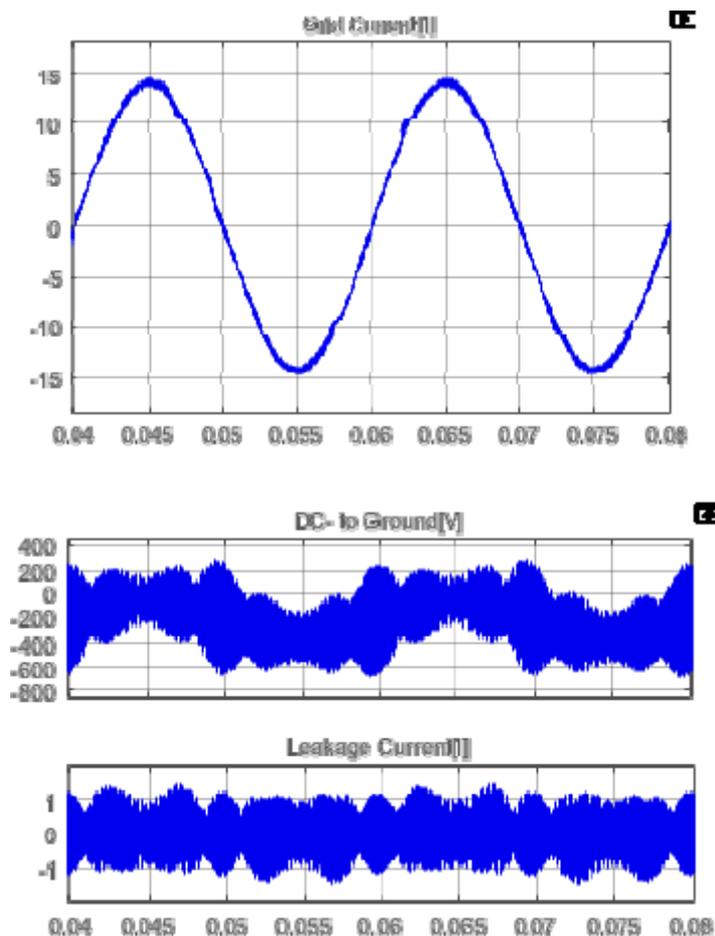


Figure 3.10: H-bridge, UPWM: load current, voltage to ground and ground leakage current

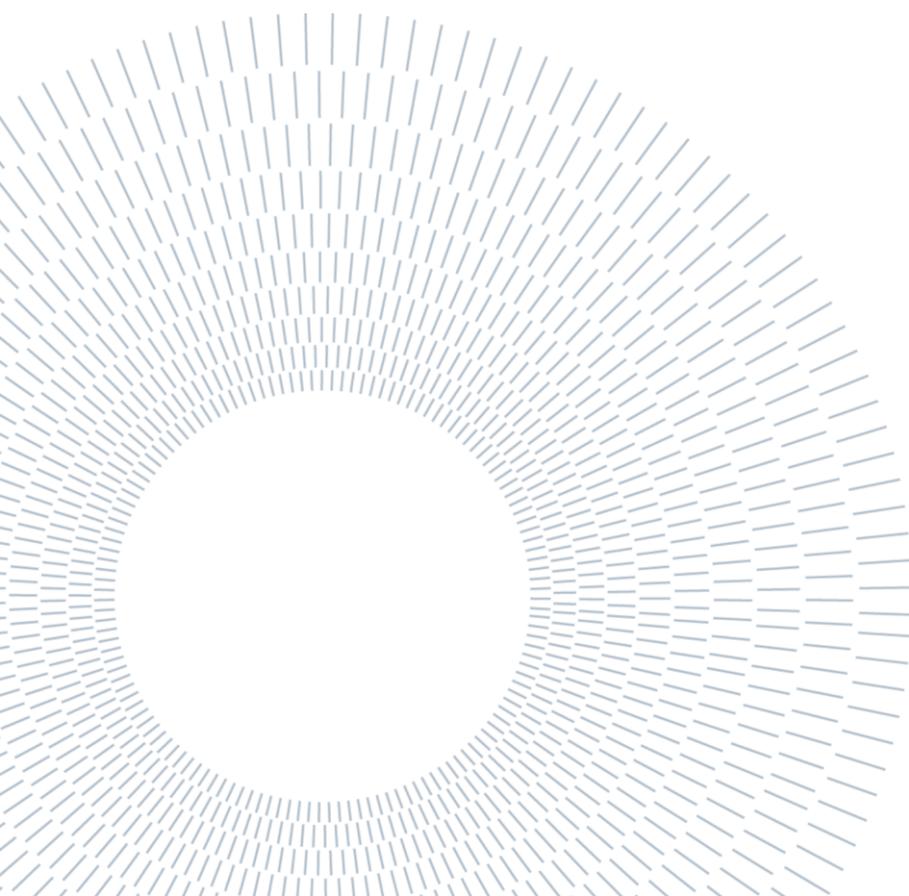
In conclusion, the transformer-less inverter requires the V_{DM} characteristics of unipolar modulation and the V_{CM} characteristics of bipolar modulation. Therefore, H5 and HERIC topologies are developed to achieve these characteristics.

This chapter evaluated the suitability of the H-bridge inverter with different modulation strategies (bipolar, and unipolar) for transformerless PV systems. While

bipolar modulation can mitigate leakage current when using a symmetrical grid filter, its low efficiency limits practical adoption.

On the other hand, Unipolar modulation introduces significant common-mode voltage, leading to high leakage current and rendering it unsuitable. The hybrid approach offers some benefits but results in square-wave voltage variations that increase leakage current and demand larger EMI filters.

Overall, none of these strategies sufficiently address the key challenges in transformerless PV applications using a standard H-bridge. These limitations motivate the introduction of advanced topologies, such as H5 and HERIC, discussed in the next chapters.



4. HERIC Inverter

4.1 HERIC Inverter Topology

The HERIC architecture consists of six switches. Four of them (S_1 to S_4) form a standard full-bridge configuration and operate at the high switching frequency. The other two auxiliary switches (S_5 and S_6) operate at the grid frequency and are used to improve the inverter's common-mode behavior. The topology of the HERIC inverter is shown in Figure 4.1 [16].

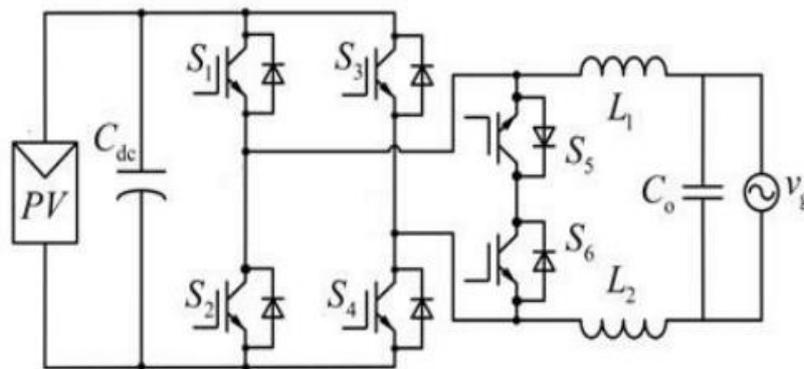


Figure 4.1: HERIC inverter topology

The HERIC inverter uses a modulation strategy similar to unipolar PWM. It utilizes two sinusoidal reference signals that are 180° out of phase. These reference signals are compared against a high-frequency triangular carrier to generate switching signals for switches S_1 , S_2 , S_3 and S_4 . As a result, the output voltage waveform resembles that of a unipolar PWM inverter as detailed in Section 1.8.2.

In HERIC topology, auxiliary switches S_5 and S_6 are used to enhance common-mode behavior and reduce leakage currents as shown in Figure 4.2.

These auxiliary switches operate during the zero-voltage vector periods, a technique known as AC decoupling. During this mode, S_5 or S_6 is activated based on the sign of the grid current, while the main switches (S_1 to S_4) are turned off. This configuration

decouples the PV array from the grid and allows the load current to freewheel, reducing switching losses and leakage. The corresponding gate signals are shown in Figure 4.2.

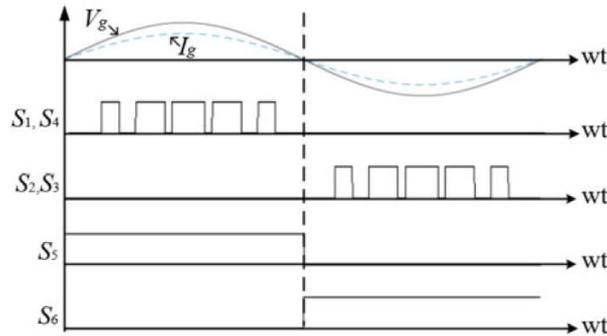


Figure 4.2: The gate signals of HERIC inverter topology

Simulation parameters, summarized in Table 4.1 and based on data from [16], shows that the HERIC inverter is highly efficient and produces minimal leakage current, making it ideal for transformerless PV systems as shown in Figure 4.3.

Table 4.1 : Simulation Parameters

Parameters	Values
Rated Power	$P_N = 3 \text{ kW}$
Switching/Sampling frequency	$f_s = 15 \text{ kHz}$
Grid frequency	$f_g = 50 \text{ Hz}$
DC-side Voltage	$V_{dc} = 400 \text{ V}$
Grid side AC voltage (RMS)	$V_g = 220 \text{ V}$
Filter capacitance	$C = 10 \text{ }\mu\text{F}$
Damping resistor	$R_C = 4.1 \text{ Ohm}$
Filter inductance (inverter side)	$L_{fi} = 2.4 \text{ mH}$
Inductance ESR (inverter side)	$R_i = 1.2 \text{ Ohm}$
Filter inductance (grid side)	$L_{fg} = 1 \text{ mH}$
Inductance ESR (grid side)	$R_g = 0.5 \text{ Ohm}$
Stray capacitance	$C_{G-PV} = 0.3 \text{ }\mu\text{F}$

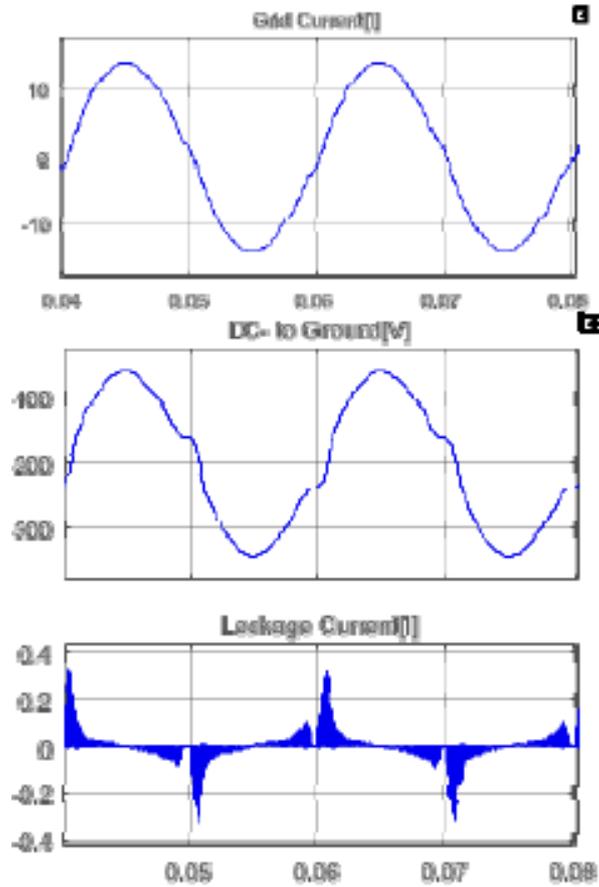


Figure 4.3: load current, voltage to ground and H-bridge, and ground leakage current

4.2 HERIC Operational Principle

In the first mode, switches S1 and S4 are turned ON during the positive half cycle of the grid voltage, therefore enabling the current to flow from the PV source via S1, then via inductor L_1 , into the grid, via L_2 , S4, and lastly back to the PV source as shown in Figure 4.4. This generates an active vector and allows power transfer to the grid where the voltages values are represented in Equation (4.1) [18].

$$\begin{cases} V_{AN} = V_{pv} \\ V_{BN} = 0 \\ V_{CM} = \frac{V_{pv}}{2} \\ V_{DM} = V_{pv} \end{cases} \quad (4.1)$$

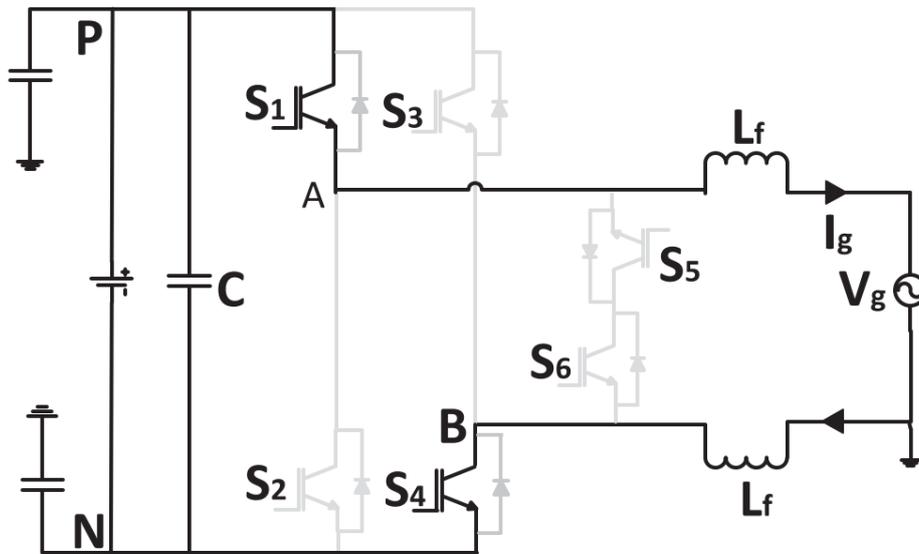


Figure 4.4: First mode of operation of HERIC inverter

Figure 4.5 demonstrates the second mode which represent the freewheeling of the positive cycle. In this state, the main switches S1, S2, S3 and S4 are turned OFF, while the auxiliary decoupling switch S5 and S6 are ON. The grid current flows through switch S5 and the antiparallel diode D6, therefore sustaining freewheel within the circuit.

During this mode, the midpoints of the inverter legs, points A and B, are both electrically floating and separated from the DC link. Due to circuit symmetry and the absence of any current injection from the DC side, these nodes stabilize at around middle potential $\frac{V_{DC}}{2}$.

This action correlates with a zero-voltage vector where the differential and common mode voltages are given in Equation (4.2) [18].

$$\begin{cases} V_{AN} = \frac{V_{pv}}{2} \\ V_{BN} = \frac{V_{pv}}{2} \\ V_{CM} = \frac{V_{pv}}{2} \\ V_{DM} = 0 \end{cases} \quad (4.2)$$

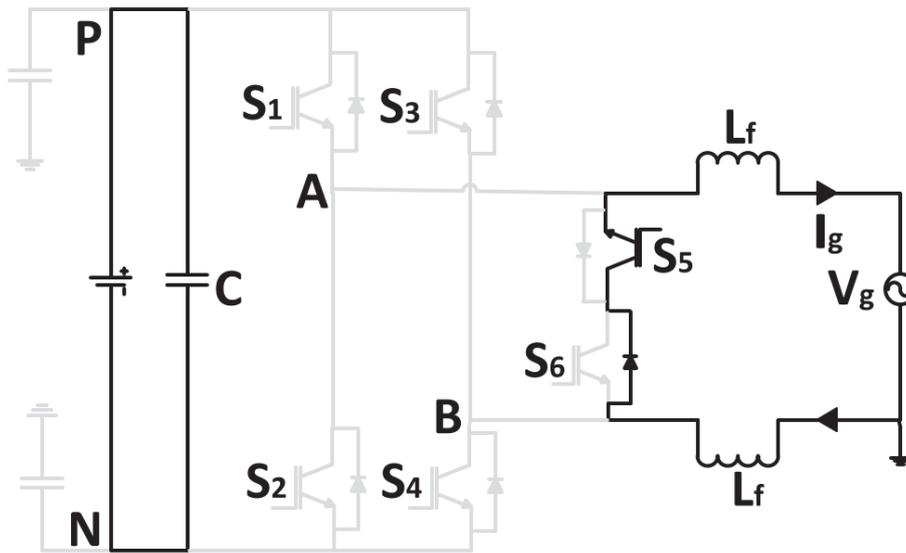


Figure 4.5: Second mode of operation of HERIC inverter

In third mode, switches S3 and S2 are switched ON during the negative half cycle. This lets the current pass from the PV source via S3, via the inductor L2, onto the grid via inductor L1, back to the PV via S2 as presented in Figure 4.6. The voltages profile is represented in Equation (4.3).

$$\begin{cases} V_{AN} = V_{pv} \\ V_{BN} = 0 \\ V_{CM} = \frac{V_{pv}}{2} \\ V_{DM} = -V_{pv} \end{cases} \quad (4.3)$$

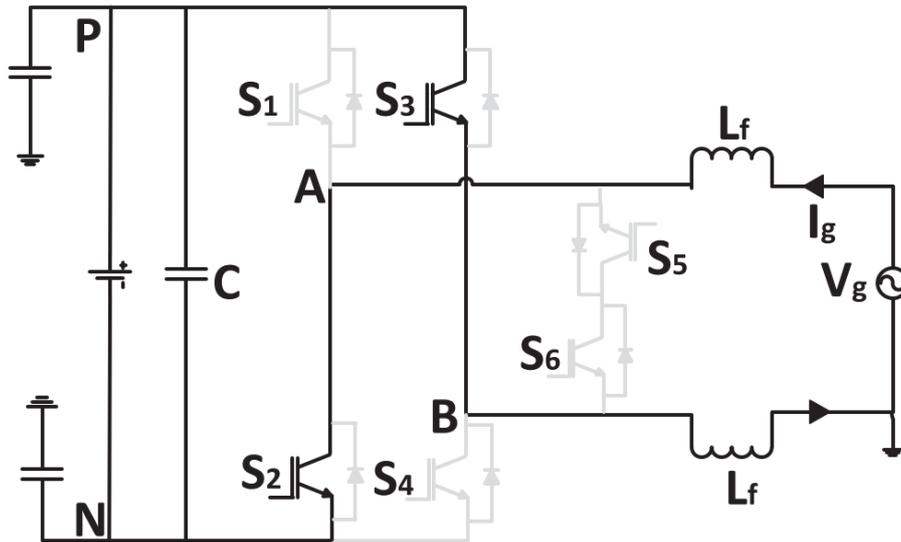


Figure 4.6: Third mode of operation of HERIC inverter

Figure 4.7 illustrates Mode 4 of the HERIC inverter, which occurs during the freewheeling interval of the negative half-cycle. In this mode, the main switches S1, S2, S3 and S4 are turned OFF, while current freewheels through switch S5 and the antiparallel diode of S6. This results in a zero-voltage vector, as no power is delivered to the grid.

Similar to Mode 2, the inverter leg midpoints A and B are disconnected from the DC link and naturally float to the midpoint potential due to the circuit's symmetry and the absence of a direct current path. Therefore, the voltages profile is presented in Equation (4.4).

$$\begin{cases} V_{AN} = \frac{V_{pv}}{2} \\ V_{BN} = \frac{V_{pv}}{2} \\ V_{CM} = \frac{V_{pv}}{2} \\ V_{DM} = 0 \end{cases} \quad (4.4)$$

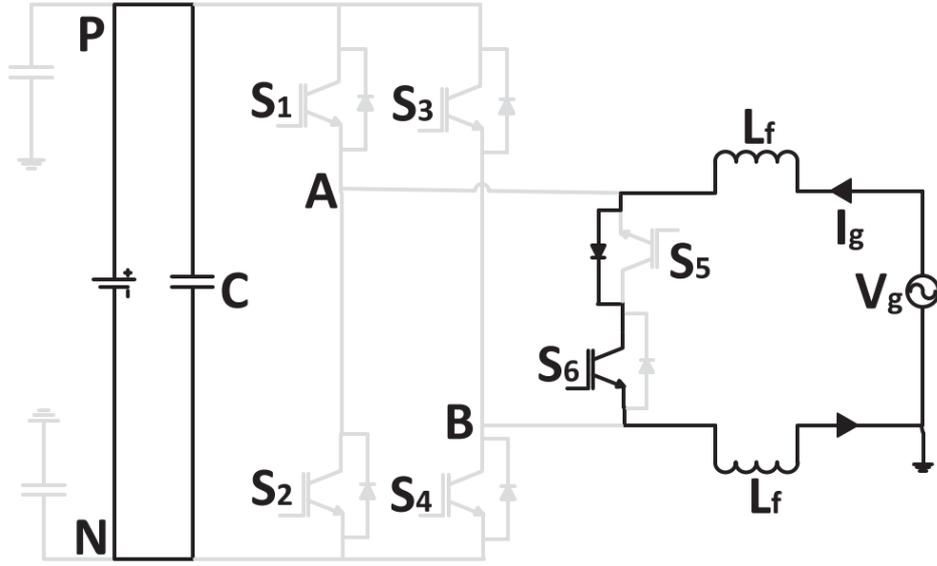


Figure 4.7: Fourth mode of operation of HERIC inverter

Table 4.2: Conduction states for HERIC inverter

Mode	S1	S2	S3	S4	S5	S6	V_{AN}	V_{BN}	V_{DM}	V_{CM}
1	ON	OFF	OFF	ON	ON	OFF	V_{pv}	0	V_{pv}	$\frac{V_{pv}}{2}$
2	OFF	OFF	OFF	OFF	ON	OFF	$\frac{V_{pv}}{2}$	$\frac{V_{pv}}{2}$	0	$\frac{V_{pv}}{2}$
3	OFF	ON	ON	OFF	OFF	ON	0	V_{pv}	$-V_{pv}$	$\frac{V_{pv}}{2}$
4	OFF	OFF	OFF	OFF	OFF	ON	$\frac{V_{pv}}{2}$	$\frac{V_{pv}}{2}$	0	$\frac{V_{pv}}{2}$

In Table (4.2), V_{DM} represents the output voltage across the inverter terminals A and B $V_{DM} = V_{AB}$ and, the V_{pv} corresponds to the input voltage from the PV array.

In conclusion, this operational sequence guarantees effective energy conversion and grid synchronization, essential for the stable functioning of grid- PV connected. In the unipolar PWM (UPWM) strategy, the inverter output voltage switches between three levels: $+V_{pv}$, 0, and $-V_{pv}$ over a complete fundamental cycle, while maintaining a constant common mode voltage $\frac{V_{pv}}{2}$. Hence, the leakage current is suppressed.

4.3 Analyzing Transition States

4.3.1 Active Power Transfer (Positive Half-Cycle)

During the positive half-cycle of grid current, switches S1, S4, and S5 are turned ON to conduct the inductor current to the grid. The remaining switches S2, S3, and S6 are OFF. In this mode, the output voltage V_{AB} equals $+V_{pv}$, and the terminal voltages V_{AN} and V_{BN} are defined by the positions of the switching nodes A and B.

4.3.2 Transition to Freewheeling State

When the HERIC inverter passes to the freewheeling state, S1 and S4 are deactivated, while S6 is activated. Nevertheless, the anti-parallel diode of S6 does not conduct instantaneously. In this transient phase, the parasitic junction capacitors linked to the switches shows dynamic behavior, Cs1 and Cs4 start charging and Cs2, Cs3, and Cs6 start discharging.

This leads to a reduction in voltage at terminal V_{AN} and an increase in V_{BN} , as energy is transferred between the capacitors. This capacitor voltage exchange temporarily modifies the common-mode voltage.

Figure 4.8 shows the charging and discharging process, and Figure 4.9 shows the initial voltages of the parasitic capacitors [19].

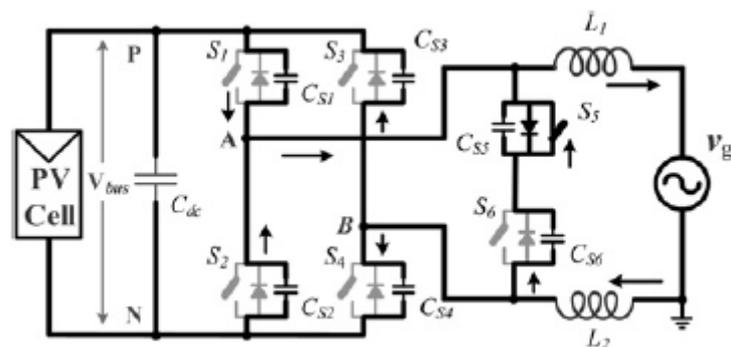


Figure 4.8: Transient charging and discharging operations

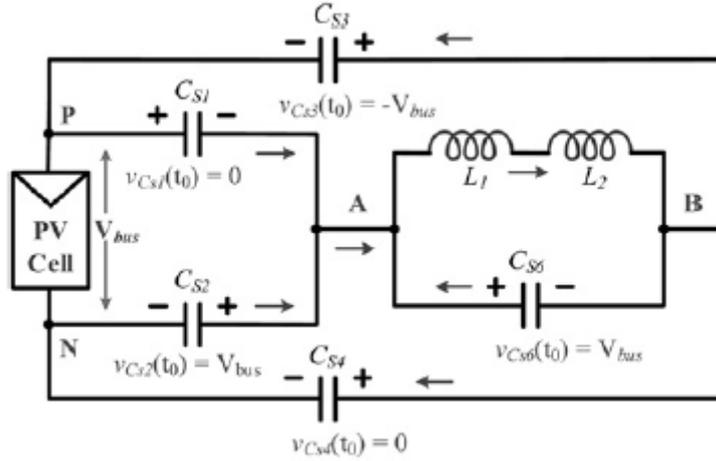


Figure 4.9: Equivalent circuit during transient operation

The anti-parallel diode of S6 does not short-circuit terminals A and B. Instead, it provides a unidirectional current path during the transition to the freewheeling state. Once it conducts, it enables current to circulate through the load and the auxiliary path, allowing terminal voltages to stabilize without directly shorting A and B. The voltage difference across A and B remains defined by the capacitor charge distribution, as expressed in Equation (4.5).

$$V_{AN} = V_{BN} = \frac{C_{S1} + C_{S3}}{C_{S1} + C_{S2} + C_{S3} + C_{S4}} V_{pv} \quad (4.5)$$

If the junction capacitors are symmetrically matched such that:

$$C_{S1} + C_{S3} = C_{S2} + C_{S4} \quad (4.6)$$

then both,

$$V_{AN} = V_{BN} = \frac{V_{pv}}{2} \quad \text{and} \quad V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{V_{pv}}{2} \quad (4.7)$$

This is the same as in the active power delivery stage, it shows that the common-mode voltage remains constant, which is critical for suppressing high-frequency leakage currents.

In the practical design, there is a mismatching for parasitic junction capacitors because of tolerances of manufacturing and the difference of material in the semiconductors. Therefore, this mismatch causes the imbalanced terminal voltages and common-mode voltage variations and leakage current.

Therefore, ensuring capacitor symmetry $C_{S1} + C_{S3} = C_{S2} + C_{S4}$ is a key design guideline to minimize leakage current in HERIC inverters.

4.3.3 Steady Freewheeling Stage Behavior:

In the steady freewheeling state, only switch S5 remains ON, while the rest of the switches are OFF. As a result, inverter terminals A and B are left floating, forming a resonant circuit between the output inductors and the parasitic capacitances of the power switches. This configuration allows a high-frequency resonance to develop, which leads to the generation of leakage current even when the common-mode voltage remains constant. This resonant path is illustrated in figure 4.10 [19, 20].

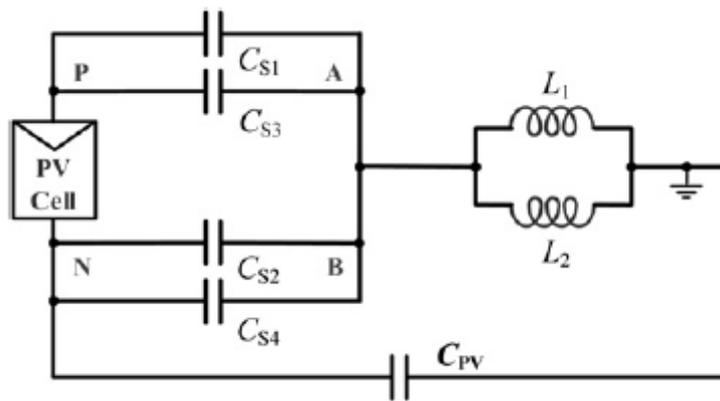


Figure 4.10: Resonant path during steady freewheeling stage

The resonance frequency is expressed as:

$$f_r = \frac{1}{2 \pi \sqrt{L_{eq} \cdot C_{eq}}} \tag{4.8}$$

With:

$$L_{eq} = \frac{L_1.L_2}{L_1+L_2} \quad (4.9)$$

The equivalent capacitance C_{eq} is expressed in Equation (4.10). It results from the series connection between the parasitic capacitance of the PV panel to ground C_{PV} , and the parallel combination of the parasitic capacitance of the inverter switches (C_{S1}, C_{S2}, C_{S3} , and C_{S4}).

$$C_{eq} = \frac{(C_{S1} + C_{S2} + C_{S3} + C_{S4})C_{PV}}{C_{S1} + C_{S2} + C_{S3} + C_{S4} + C_{pv}} \quad (4.10)$$

Since the PV-ground parasitic capacitance C_{pv} is typically larger than the junction capacitances of the switches, the equivalent capacitance can be approximated as presented in Equation (4.11).

$$C_{eq} \approx C_{S1} + C_{S2} + C_{S3} + C_{S4} \quad (4.11)$$

This means that, due to resonance between these non-ideal elements, the HERIC inverter cannot completely suppress leakage current, even during steady-state operation.

5. H5 Inverter

5.1 H5 Inverter Topology

When a full H-bridge transformerless inverter is used, an undesirable common-mode voltage (CMV) often appears. This fluctuating common-mode voltage (CMV) can cause leakage currents through a parasitic circuit formed by the stray capacitance between the PV array and ground.

To address this issue, the H5 inverter topology modifies the standard full H-bridge by adding an additional switch, Q_5 , between the DC input and the H-bridge as shown in Figure 5.1. For DC decoupling states to be guaranteed, the added switch Q_5 commutes at the switching frequency. As shown in Figure 5.2, which shows the output voltage waveform and the corresponding gate signals for switches Q_1 to Q_5 during one full cycle of operation [21, 22].

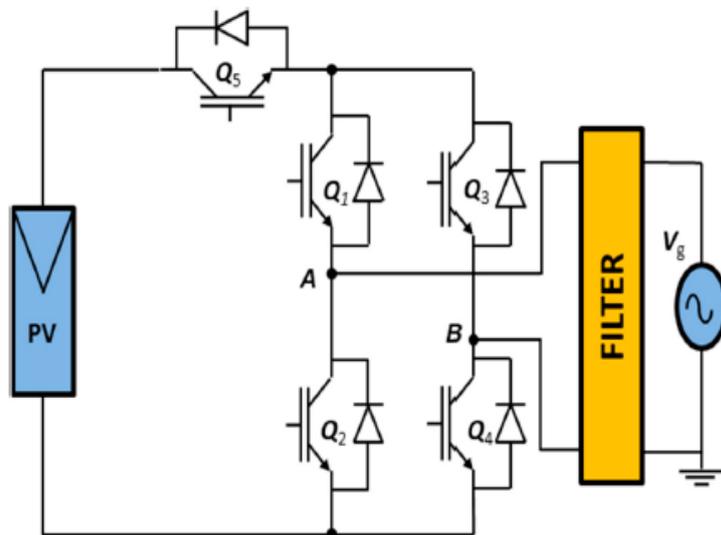


Figure 5.1: H5 inverter topology

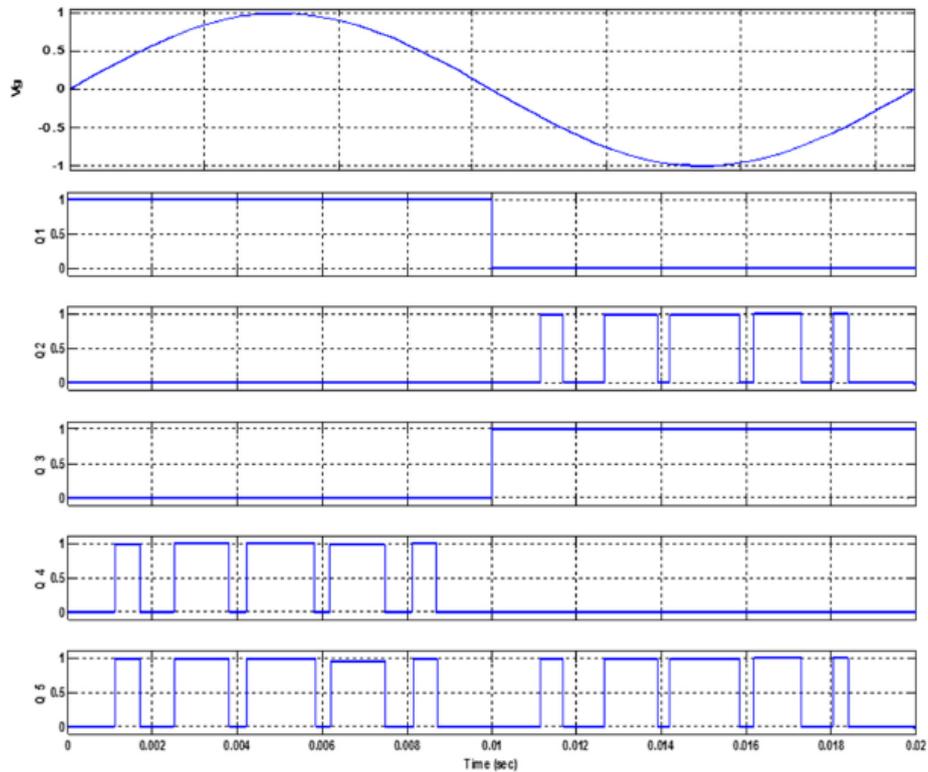


Figure 5.2: Control signals of H5 inverter switches

In the first operating mode, switch S1 remains continuously on, while switches S4 and S5 commute at the switching frequency, directing the current flow through switches S1, S4, and S5 as demonstrated Figure 5.3. This results in an output voltage $V_{AB} = +V_{pv}$. The corresponding common-mode voltage (VCM) during this mode can be calculated using the following expression:

$$V_{CM} = \frac{1}{2} (V_{AN} + V_{BN}) = \frac{1}{2} (V_{PV} + 0) = \frac{V_{PV}}{2} \quad (5.1)$$

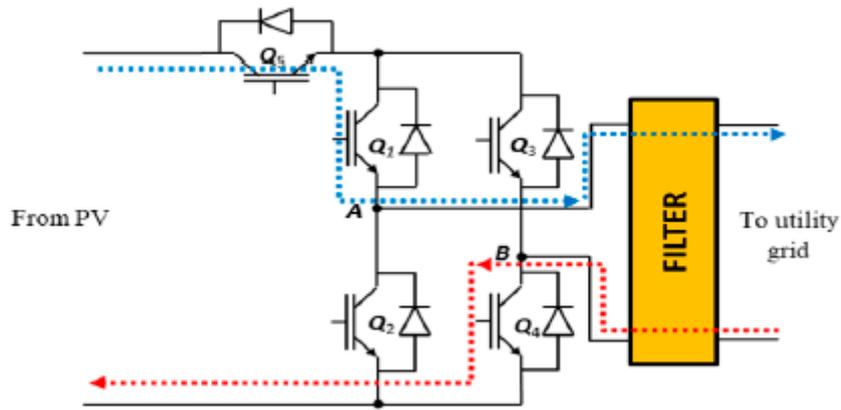


Figure 5.3: first mode, Pathway of the H5 in the positive voltage vector

In the second mode, switches S4 and S5 are turned off, resulting in a drop in the inductor current, which now flows through switch S1 and the body diode of S3 as shown in Figure 5.4. The output voltage in this mode is $V_{AB} = 0$. The common-mode voltage V_{CM} can be determined using the following equation:

$$V_{CM} = \frac{1}{2}(V_{AN} + V_{BN}) = \frac{1}{2}\left(\frac{V_{PV}}{2} + \frac{V_{PV}}{2}\right) = \frac{V_{PV}}{2} \quad (5.2)$$

In the freewheeling state, both nodes A and B are floating and not actively driven by the inverter legs. Due to the symmetrical structure of the bridge and capacitive voltage division across the switches, both nodes settle at an average potential of $\frac{V_{PV}}{2}$ that leads to $V_{AN} = V_{BN} = \frac{V_{PV}}{2}$.

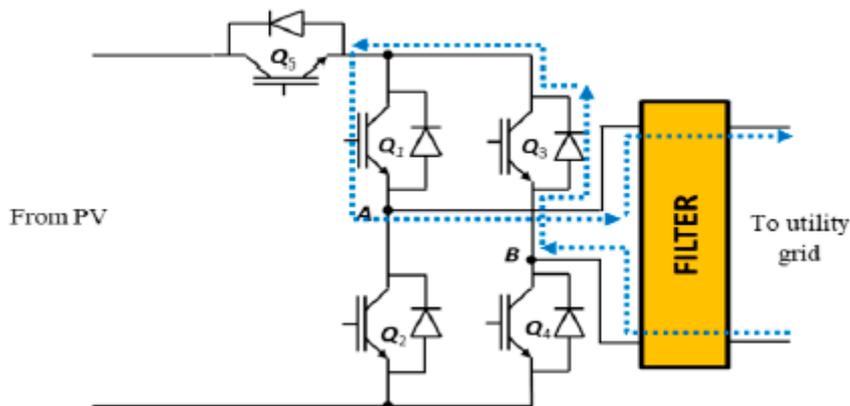


Figure 5.4: Second mode, Pathway of the H5 in the freewheeling - Positive Cycle

Figure 5.5 illustrates the third mode of operation. Similar to the first mode, switches S2 and S5 commute at the switching frequency, while switch S3 remains continuously on during the negative half-cycle. This results in a reverse increase in the inductor current. In this case $V_{AN} = 0$ while $V_{BN} = V_{pv}$.

Therefore, V_{CM} and V_{DM} are given by Equation (5.3).

The common-mode voltage (V_{CM}) can be calculated using the following expression:

$$\begin{cases} V_{AN} = 0 \\ V_{BN} = V_{pv} \\ V_{DM} = -V_{pv} \\ V_{CM} = \left(\frac{V_{PV}}{2}\right) \end{cases} \quad (5.3)$$

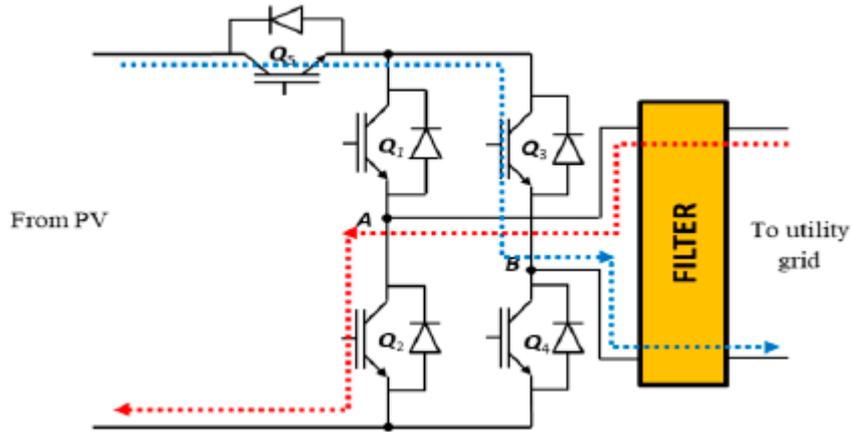


Figure 5.5: third mode, Pathway of the $H5$ in the negative vector

In the fourth mode, during the negative half-cycle of the grid current, switches S2 and S5 are turned off, initiating the freewheeling mode. In this state, voltage V_{BN} decreases while voltage V_{AN} increases until they reach the same value as shown in Figure 5.6.

As a result, the output voltage becomes $V_{AB} = 0$, and the inductor current flows through switch S3 and the body diode of S1, similar to the behavior observed in second mode. The common-mode voltage V_{CM} for this mode is calculated using the following expression:

$$V_{CM} = \frac{1}{2}(V_{AN} + V_{BN}) = \frac{1}{2}\left(\frac{V_{PV}}{2} + \frac{V_{PV}}{2}\right) = \frac{V_{PV}}{2} \quad (5.4)$$

Since both legs of the inverter are inactive, nodes A and B are floating. Due to the symmetrical configuration and capacitive effects in the bridge, the voltages at both nodes stabilize around the midpoint of the DC bus. This results in $V_{AN} = V_{BN} = \frac{V_{PV}}{2}$, which leads to a constant common-mode voltage $V_{CM} = \frac{V_{PV}}{2}$, as shown in Equation (5.4).

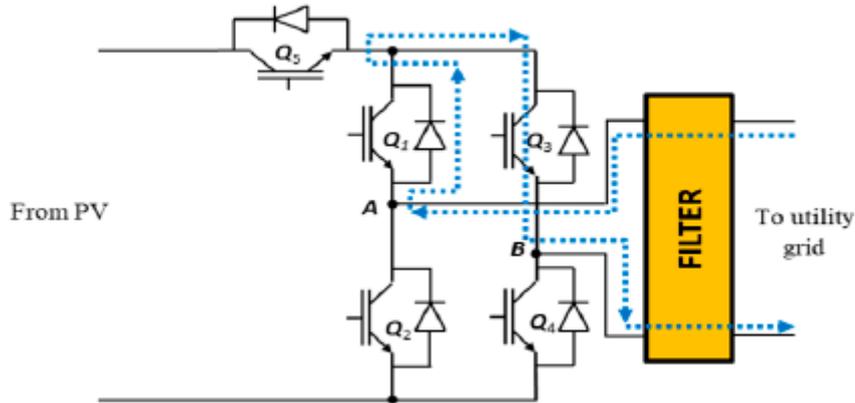


Figure 5.6: Fourth mode, Pathway of the H5 in the freewheeling – Negative Cycle

Table 5.1: Conduction states for H5 inverter

Mode	S1	S2	S3	S4	S5	V_{AN}	V_{BN}	V_{DM}	V_{CM}
1	ON	OFF	OFF	ON	ON	V_{pv}	0	V_{pv}	$\frac{V_{pv}}{2}$
2	ON	OFF	OFF	OFF	OFF	$\frac{V_{pv}}{2}$	$\frac{V_{pv}}{2}$	0	$\frac{V_{pv}}{2}$
3	OFF	ON	ON	OFF	ON	0	V_{pv}	$-V_{pv}$	$\frac{V_{pv}}{2}$
4	OFF	OFF	ON	OFF	OFF	$\frac{V_{pv}}{2}$	$\frac{V_{pv}}{2}$	0	$\frac{V_{pv}}{2}$

In Table (5.1), V_{DM} represents the output voltage across the inverter terminals A and B $V_{DM} = V_{AB}$ and, the V_{pv} corresponds to the input voltage from the PV array.

In conclusion, throughout the four defined commutation modes, the common-mode voltage remains approximately constant, with $V_{CM} = \frac{1}{2} V_{PV}$. This consistency demonstrates that the improved H5 inverter architecture, when employing Unipolar Sinusoidal Pulse Width Modulation (USPWM), is capable of effectively maintaining a stable CM voltage across all operational modes.

According to the simulation listed in the Table (4.1), the H5 inverter is highly efficient and produces minimal leakage current, making it ideal for transformerless PV systems as shown in Figure 5.7 [16].

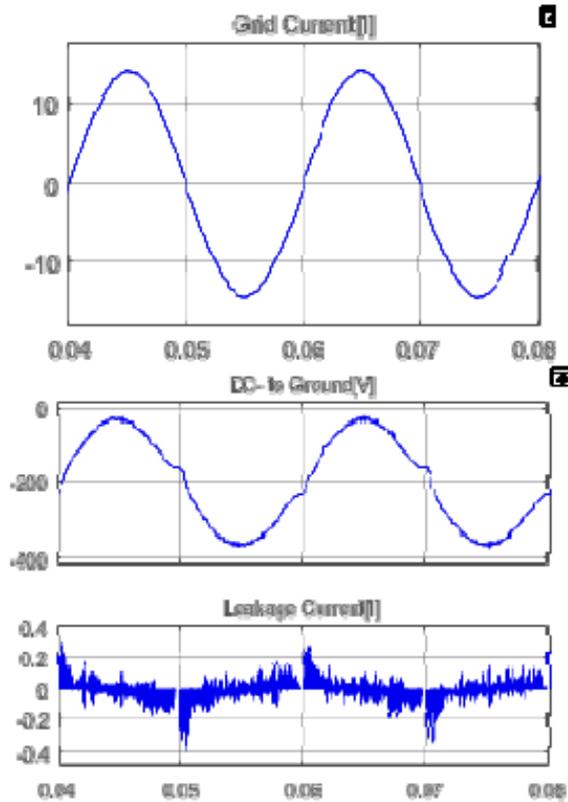


Figure 5.7: load current, voltage to ground and ground leakage current for H5

5.2 | The enhanced H5 inverter topology

5.2.1 Circuit structure of the improved H5 topology

Figure 5.8 shows the advanced H5 inverter design that results in several improvements at improving the efficiency and effectiveness of grid-connected photovoltaic (PV) systems. In the enhanced design, MOSFETs replace conventional high-frequency IGBTs in each phase leg, delivering superior switching performance [21].

Furthermore, switches S2 and S4 are connected with two additional capacitors to help further suppress common-mode leakage currents. For having a smooth output from inverter and before injecting to grid integration, inductors L_A and L_B , along with capacitor C_O , are configured as an LC filter.

This improved configuration enables the implementation of Unipolar Sinusoidal Pulse Width Modulation (SPWM), allowing for the generation of a three-level output voltage while consistently maintaining a stable common-mode (CM) voltage during operation.

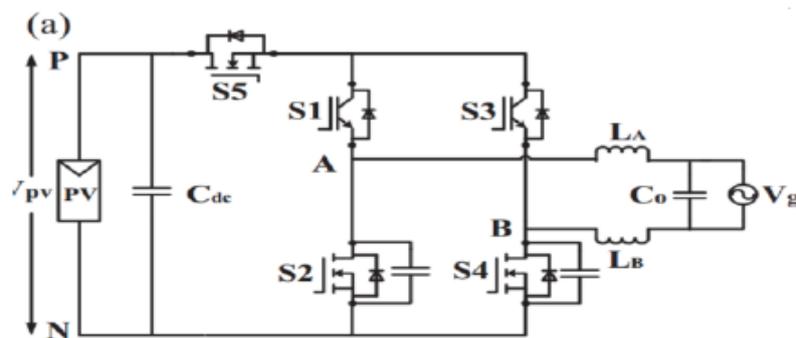


Figure 5.8: The improved H5 inverter topology

5.3 Impact of junction capacitance:

In practical inverter systems, parasitic capacitances that are modeled as small capacitors have a significant effect on the behavior of voltage transitions during switching events.

When the inverter shifts from first active modes to the freewheeling modes, the capacitance affects the voltages during switching. This results in non-ideal common-mode voltage behavior and also high-frequency leakage currents.

During active mode, the photovoltaic (PV) array is directly connected to the grid through the output filter inductors. This coupling makes the effect of junction capacitance on common mode voltage relatively insignificant. However, in freewheeling modes, switch S5 opens and isolates the PV array from the grid. In this decoupled state, the inverter's behavior becomes much more sensitive to the junction capacitances of the switches, making leakage current suppression more challenging.

5.4 Analyzing Transition States

5.4.1 Phase I – Transient Capacitance Exchange:

During the commutation from Mode I to Mode II, an equivalent transient circuit can be derived, as illustrated in Figure 5.9 [22].

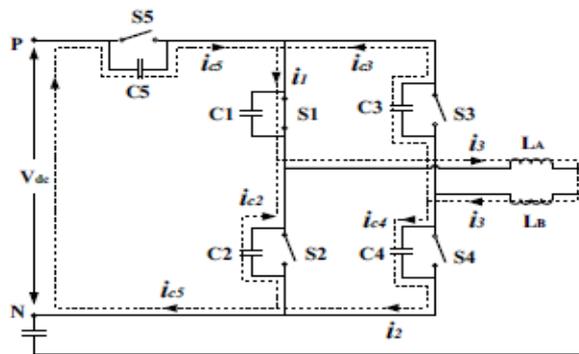


Figure 5.9: Transient circuit by considering the switching from mode I to mode II

C_1 through C_5 shows the junction capacitances of the switches S1 to S5, respectively. The transient charging and discharging phenomena are done by the junction capacitors C_2 , C_3 , C_4 , and C_5 , which become active when switches S4 and S5 are switched off, but before the body diode of switch S3 begins conducting to support the freewheeling current.

By using the Kirchhoff's Current Law (KCL) to the circuit, the following current relationships are shown in Equations 5.5, 5.6 and 5.7:

$$i_1 = i_{c3} + i_{c5} \quad (5.5)$$

$$i_2 = i_{c4} = i_{c2} + i_{c5} \quad (5.6)$$

$$i_3 = i_{c2} + i_{c3} + i_{c5} \quad (5.7)$$

Equation 5.5, the inductor current i_1 , which previously flowed through S4 and S5, now splits and charges the parasitic capacitances C_3 and C_5 after the switches turn off

Equation 5.6 shows the current i_2 flowing into the branch with C_4 , is the result of two charging paths through C_2 and C_5 which are now connected in parallel due to the switching state.

Equation 5.7 shows that the current i_3 charging C_2 is the result of the combined currents from C_3 and C_5 , again due to the interconnection of the capacitors in this transient period.

i_1 , i_2 , and i_3 represent the total charging or discharging currents. i_{c2} , i_{c3} , i_{c4} , and i_{c5} show the individual currents through the corresponding capacitors.

As shown in the equivalent transient model in Figure 5.10, during this phase, the Capacitor C_4 is charged by the parallel combination of C_2 and C_5 . And, this charging occurs through the output filter inductors L_A and L_B . Consequently, the voltage across C_4 increases, while the voltage across C_2 decreases until both voltages become equal.

V_{PV} is the overall DC-link voltage across the PV array, whereas V_{AN} and V_{BN} stand for the voltages at the inverter's output nodes A and B (relative to the midpoint or neutral of the DC link) in Figure 5.9. these nodes correspond to the inverter AC terminals connected to the grid through filter inductors L_A and L_B .

Based on charge conservation theory, the voltage at nodes V_{AN} and V_{BN} during this transient state is expressed as (5.8):

The corresponding transient circuit in Figure 5.10, where capacitor C_4 is charged by the parallel combination of C_2 and C_5 via the output filter inductors L_A and L_B , is used to get this expression. The total initial charge stored in C_2 and C_5 (at voltage V_{pv}) is conserved if perfect capacitors and no losses are present. Consequently, the final common-mode voltage across all three capacitors, using charge conservation, is:

$$V_{AN} = V_{BN} = V_{PV} \left(\frac{C_2 + C_5}{C_2 + C_4 + C_5} \right) \quad (5.8)$$

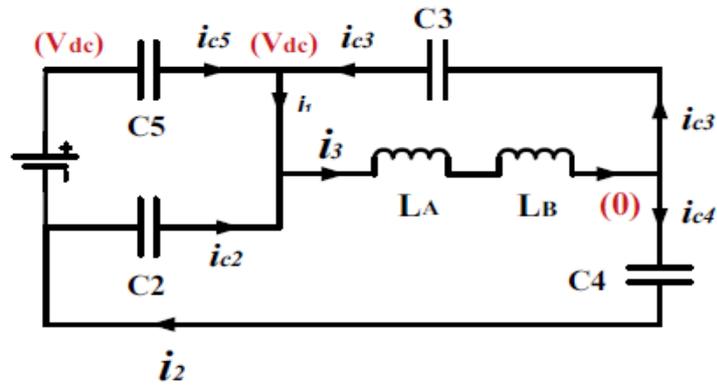


Figure 5.10: simplified circuit

5.4.2 Phase II – Freewheeling Begins:

Once the body diode of switch S3 starts conducting, the freewheeling state begins, marking the end of the transient period. As described by Equation (5.6), the common-mode voltage (V_{CM}) reaches its ideal value $V_{CM} = \frac{V_{PV}}{2}$ only if the condition $C_4 = C_2 + C_5$ is satisfied at the end of the transient phase. This ensures stable voltages at both V_{AN} and V_{BN} , and thereby prevents the generation of leakage current.

However, if this condition is not met (i.e., $C_4 \neq C_2 + C_5$), the voltages V_{AN} , V_{BN} and consequently V_{CM} will deviate from the ideal value of $\frac{V_{PV}}{2}$. This imbalance disrupts the CM voltage stability, resulting in the flow of high-frequency leakage current through the junction capacitors, parasitic capacitances, and filter inductors, as illustrated in Figure 5.11 [22].

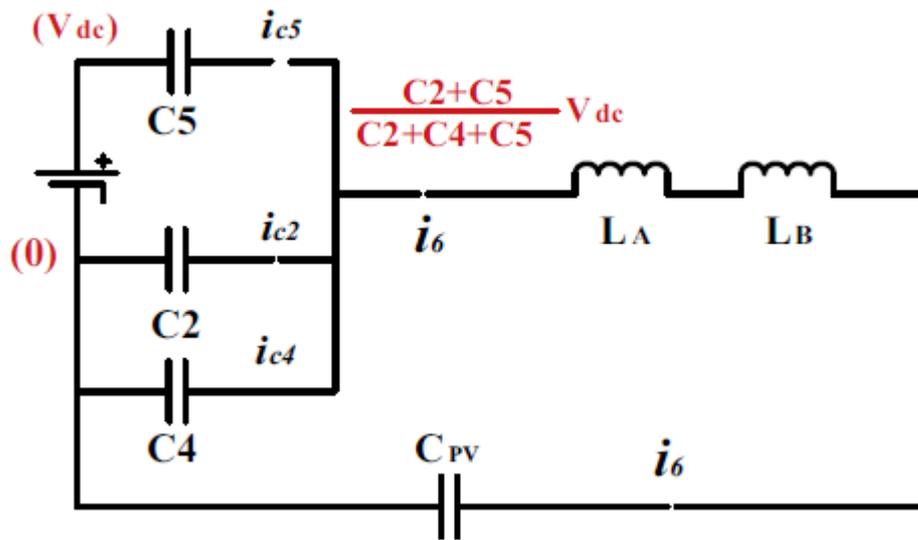


Figure 5.11: Simplified equivalent resonant circuit in mode II

In the proposed improved H5 inverter topology, there are always two key commutations from non-decoupling (active) states to decoupling (freewheeling) states:

1. Mode I \rightarrow Mode II: $C_4 = C_2 + C_5$
2. Mode III \rightarrow Mode IV: $C_2 = C_4 + C_5$

Solving these two conditions simultaneously yields the theoretical requirement for complete leakage current elimination:

$$C_5 = 0 \text{ and } C_2 = C_4$$

However, in practical applications, achieving zero junction capacitance ($C_5 = 0$) is not feasible due to the physical properties of semiconductor switches. Therefore, the theoretical condition is modified for real-world implementation as:

$$C_2 = C_4 + C_5 \quad (5.9)$$

This adjusted condition provides a practical design guideline to minimize CM voltage fluctuations and suppress leakage currents effectively.

6. Reactive Power Capability

6.1 Introduction

As discussed in the previous chapters, some topologies like H5 and HERIC with simple PWM techniques are capable of connecting PV system to the grid without a transformer while minimizing the leakage current. However, this is suitable for unity power factor meaning that reactive power support was not considered. In this chapter, a proposed modulation technique supporting reactive power capability for both H5 and HERIC is explained in detail.

6.2 Reactive Power Capability for both H5 and HERIC inverters

As mentioned previously, the reactive power needs to be studied. In this section the reactive power capability of H5 and HERIC inverters are analyzed.

The working principles of HERIC and H5 inverters operating at unity power factor are analyzed in detail in Sections 4.2 and 5.1, respectively.

It can be concluded that, for unity power factors, both H5 and HERIC inverters generate unipolar PWM while maintaining a constant common mode voltage $\frac{V_d}{2}$, thereby suppressing the leakage current.

6.2.1 Non-unity power factor

During the interval when the instantaneous power $p(t) = v_g(t)i_g(t)$ is negative, grid voltage $v_g(t)$ and grid current $i_g(t)$ have opposite signs, indicating reactive power exchange. Figure 6.1 demonstrates the operation of H5 inverter under the condition where $v_g(t)$ is negative and $i_g(t)$ is positive. In this case, the current circulates through the antiparallel diodes of the switches S5, S3 and S2 [23].

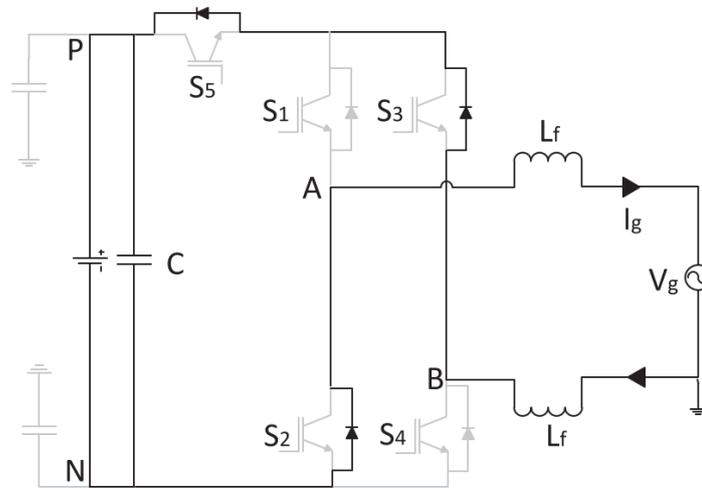


Figure 6.1: Operation modes of conventional H5 topology in negative power region. V_g is negative and I_g is positive.

Similarly, Figure 6.2 illustrates the working principles of HERIC inverter when $v_g(t)$ is negative and $i_g(t)$ is positive. The current circulates through the antiparallel diodes of the switches S2 and S3.

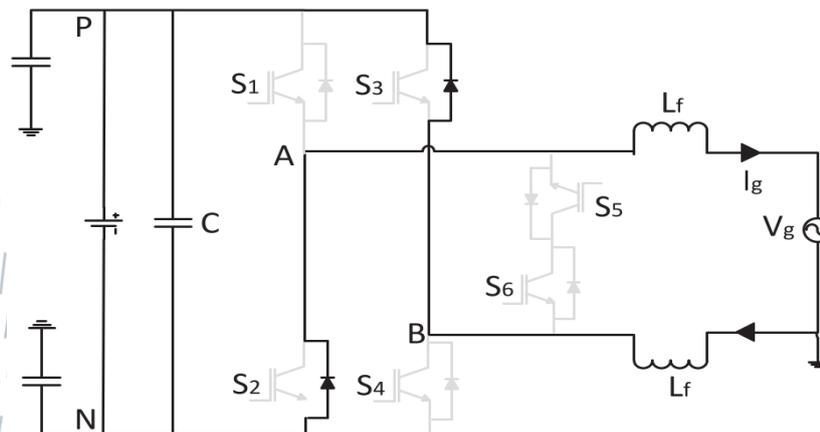


Figure 6.2: Operation modes of conventional HERIC topology in negative power region. (a) V_g is negative and I_g is positive.

Consequently, the voltage values for both H5 and HERIC inverters when V_g is negative and I_g is positive are identical and are given by Equation (6.1).

$$\begin{aligned} V_{AN} &= 0 \\ V_{BN} &= +V_{pv} \\ V_{DM} &= -V_{pv} \\ V_{CM} &= \frac{V_{pv}}{2} \end{aligned} \tag{6.1}$$

On the other hand, when V_g is positive and I_g is negative the current circulates through the antiparallel diodes of the switches S5, S1 and S4 of H5 inverter as illustrated in Figure 6.3.

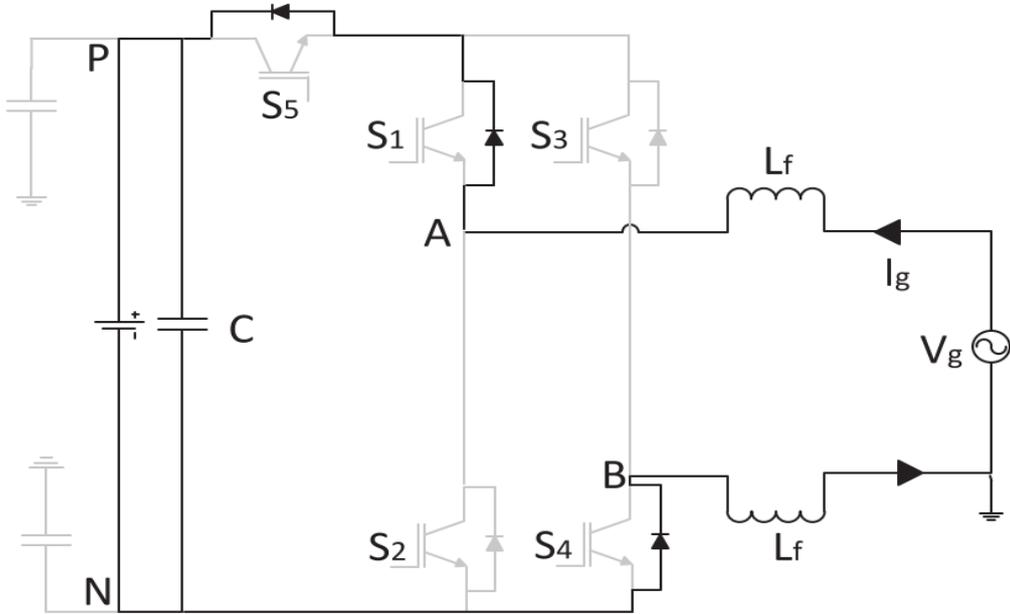


Figure 6.3: Operation modes of conventional H5 topology in negative power region. V_g is positive and I_g is negative.

Similarly, HERIC inverter operation when V_g is positive and I_g is negative is illustrated in Figure 6.4. The current freewheels through the antiparallel diodes of the switches S1 and S4.

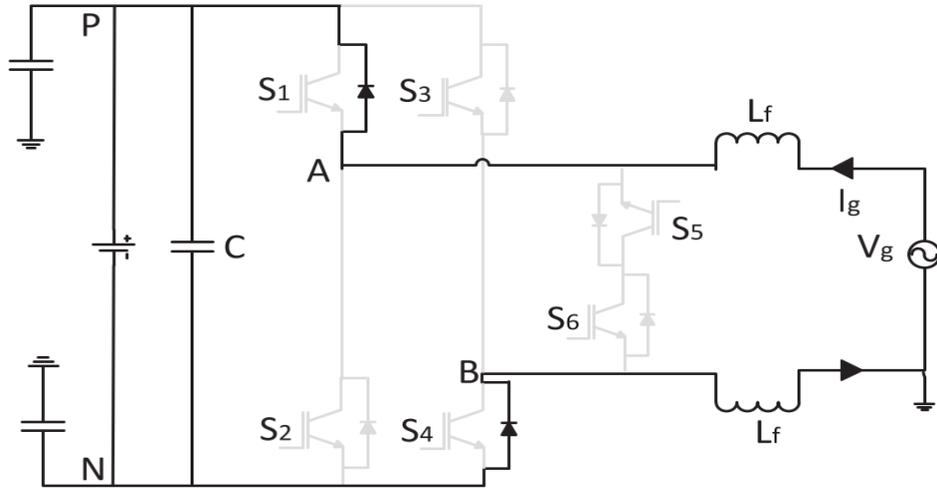


Figure 6.4: Operation modes of conventional HERIC topology in negative power region. V_g is positive and I_g is negative.

Hence, the voltage values for both H5 and HERIC inverters when V_g is positive and I_g is negative are identical and are given by Equation (6.2).

$$\begin{cases} V_{AN} = +V_{pv} \\ V_{BN} = 0 \\ V_{DM} = V_{pv} \\ V_{CM} = \frac{V_{pv}}{2} \end{cases} \quad (6.2)$$

As illustrated, for both for H5 and HERIC inverters, there is no current path that allows the generation of a zero-voltage state under traditional PWM. However, during the negative power region the current freewheels through the anti-parallel diodes producing either $+V_{pv}$ or $-V_{pv}$ as presented Equations (6.1) and (6.2). This operating performance is comparable to that of an H-Bridge with bipolar PWM, that is characterized by low efficiency, as discussed in Section 3.2.

Consequently, the H5 and HERIC inverters are not suitable for reactive power applications. They are unable to meet the requirements of current grid codes, such as those outlined in IEEE 1547 and VDE-AR-N 4105, which require that grid-connected inverters must be able to supply or absorb reactive power to support grid stability and voltage regulation even when there is no actual power flow.

6.3 A proposed Modulation Technique with Reactive Power Capability

As discussed in the previous section, conventional modulation for both H5 and HERIC does not support reactive power. Hence in the section, a proposed modulation technique is discussed. The goal of the proposed modulation is to achieve zero voltage vector within the negative power area allowing reactive power capability.

6.3.1 The proposed modulation in H5 inverter

Figure 6.5 illustrates the proposed modulation technique for the H5 inverter. Instead of switching off S1 during the negative voltage period (as is done in traditional modulation) S1 is switched complementarily to S2. This approach aims to create a new current circulation path that enables zero voltage vectors during Period III [24].

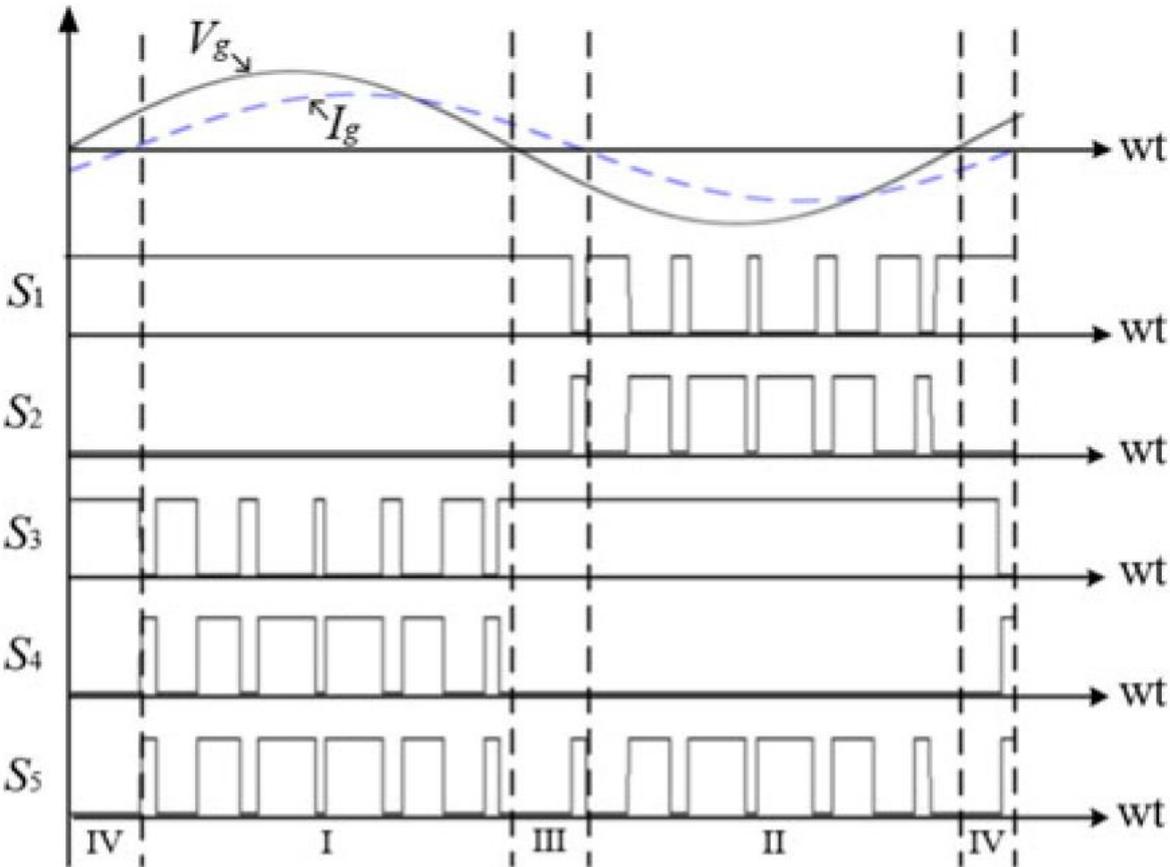


Figure 6.5: Proposed switching pattern for H5.

When S1 and S3 are ON while S2, S4, and S5 are OFF, the current circulates through the antiparallel diode of S3 and switch S1, as illustrated in Figure 6.6. Consequently, V_{AN} increases from zero, and V_{BN} decreases from V_{pv} until both reach a common value. Therefore, the differential and common-mode voltages are given by Equation (6.3) [23].

$$\begin{cases} V_{DM} = 0 \\ V_{CM} = \frac{V_d}{2} \end{cases} \quad (6.3)$$

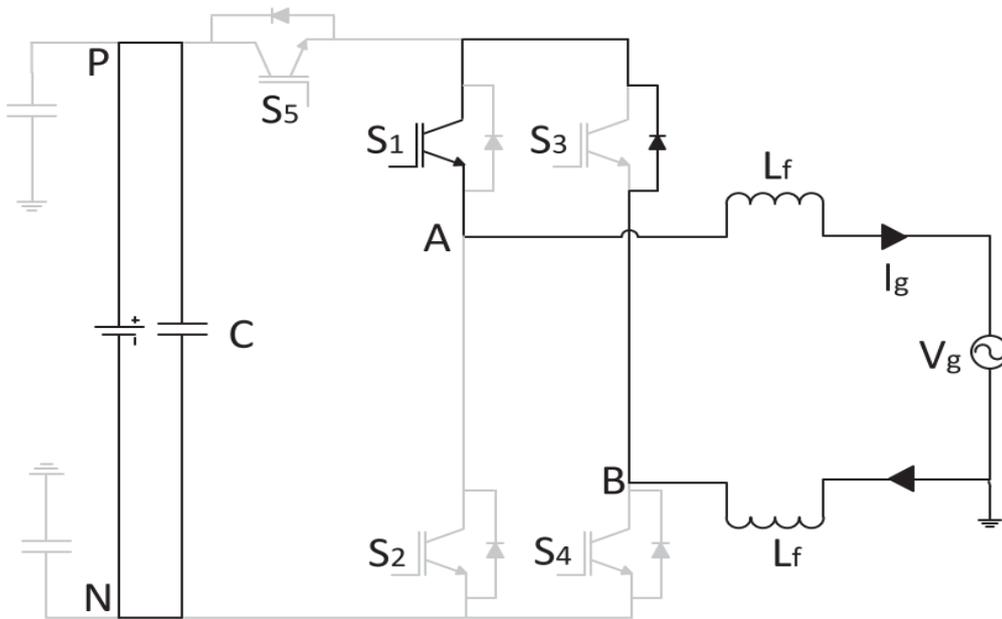


Figure 6.6: Zero-voltage state of H5 inverter with proposed PWM. V_g is negative and I_g is positive

Similarly, in Region IV (where the V_g is positive and I_g is negative) S3 switches complementarily to S4, as shown in Figure 6.5. When S1 and S3 are ON while S2, S4, and S5 are OFF, the current circulates through the antiparallel diode of S1 and switch S3, as illustrated in Figure 6.7. Consequently, V_{AN} increases from zero and V_{BN} decreases from V_{pv} until both reach a common value. Therefore, the differential and common-mode voltages are given by Equation (6.4).

$$\begin{cases} V_{DM} = 0 \\ V_{CM} = \frac{V_d}{2} \end{cases} \quad (6.4)$$

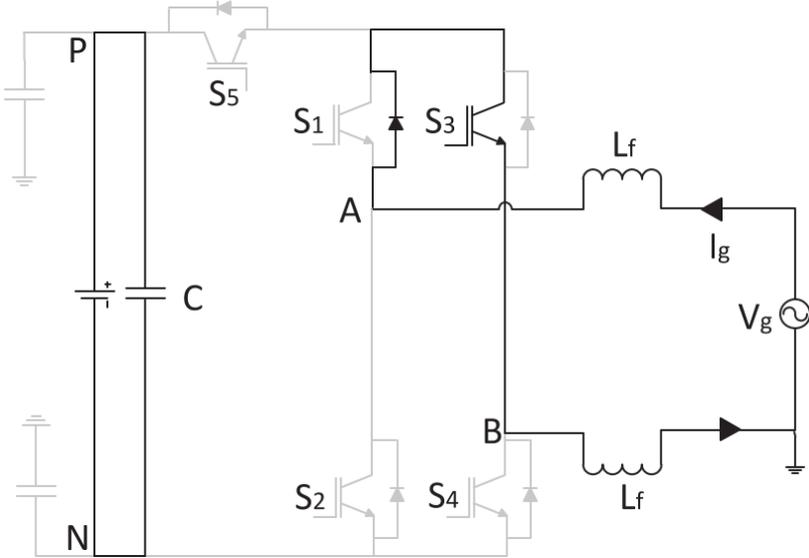


Figure 6.7: Zero-voltage state of H5 inverter with proposed PWM. V_g is positive and I_g is negative.

6.3.2 The proposed modulation in HERIC inverter

Similar to the modifications applied to the H5 inverter, Figure 6.8 illustrates the proposed modulation technique for the HERIC inverter. This technique ensures that during the freewheeling period, both S5 and S6 switches are ON.

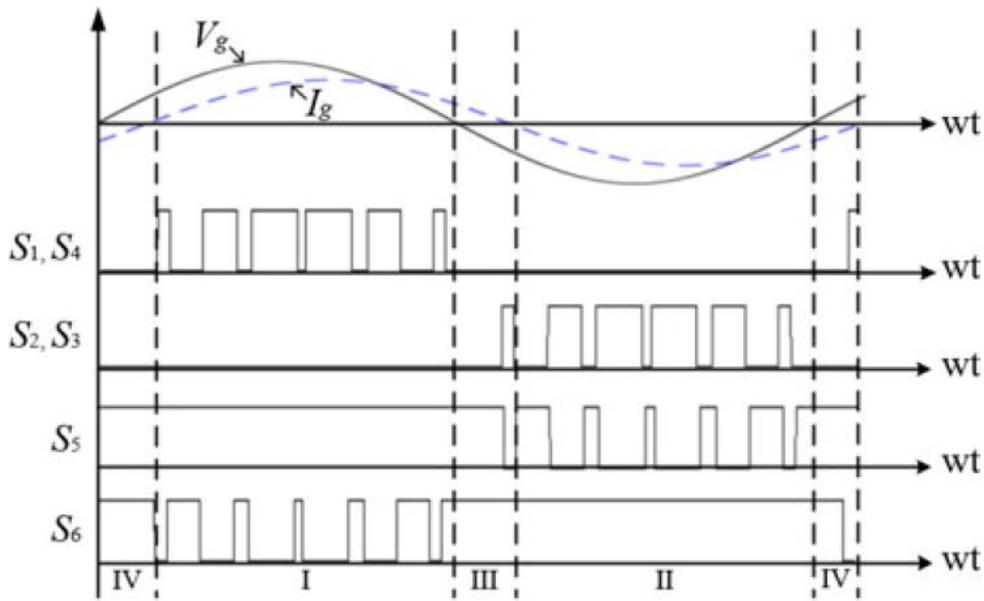


Figure 6.8: Proposed switching pattern for HERIC.

Consequently, new freewheeling current paths are established, as shown in Figure 6.9. Figure 6.9(a) illustrates the freewheeling path when V_g is negative while I_g is positive. In this case, the current circulates through the antiparallel diodes of switches S6 and S5. As a result, V_{AN} increases from zero and V_{BN} decreases from V_{pv} until both reach a common value. Therefore, the differential and common-mode voltages are given by Equation (6.5).

$$\begin{cases} V_{DM} = 0 \\ V_{CM} = \frac{V_d}{2} \end{cases} \quad (6.5)$$

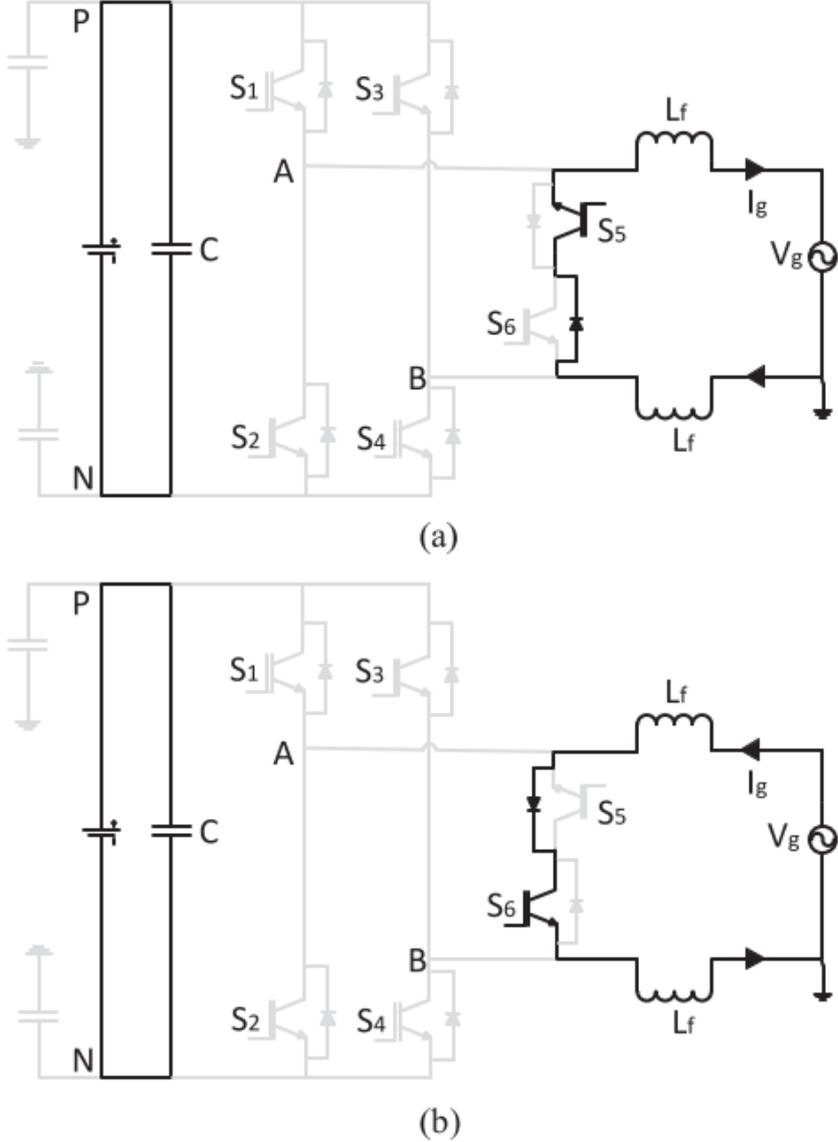


Figure 6.9: Zero-voltage state of HERIC inverter with proposed PWM. (a) V_g is negative and I_g is positive. (b) V_g is positive and I_g is negative.

Figure 6.9(b) presents the freewheeling path when V_g is positive and I_g is negative. In this case, the current circulates through the antiparallel diodes of switches S5 and S6. As a result, V_{AN} increases from zero, and V_{BN} decreases from V_{pv} until both reach a common value. Therefore, the differential and common-mode voltages are given Equation (6.6).

$$\begin{cases} V_{DM} = 0 \\ V_{CM} = \frac{V_d}{2} \end{cases} \quad (6.6)$$

To conclude, the proposed modulation strategy introduced a new current pass in the negative power region (region *III* and *IV*) achieving zero voltage state. Consequently, unipolar modulation is achieved ($+V_d, 0, -V_d$) as shown in Figure 6.10. Hence, reactive power capability is achieved for both H5 and HERIC inverters. Moreover, the leakage current is suppressed as the common mode voltage is held constant at $\frac{V_d}{2}$ along the operation. Notably, the proposed technique allows reactive power support without any changes in the inverter structure.

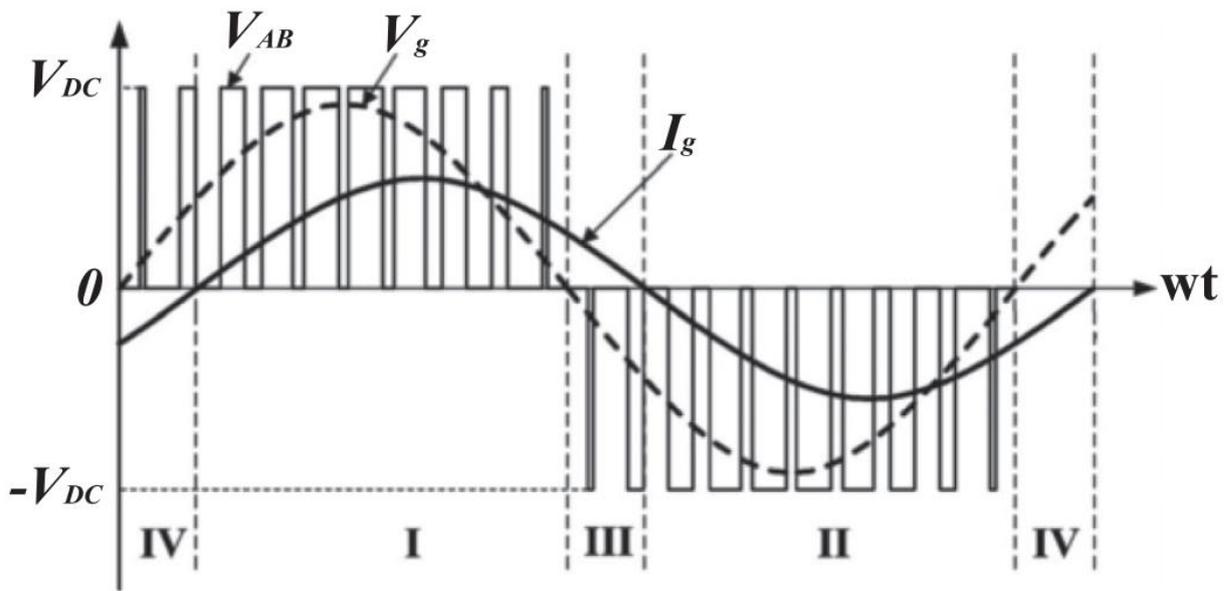


Figure 6.10: Waveforms of proposed PWM under non-unity power factor

7. Conclusion and future development

Two popular transformerless single-phase inverter topologies, HERIC and H5, in grid-connected photovoltaic (PV) systems have been thoroughly analyzed and contrasted in this thesis. The main goal was to solve the crucial problem of leakage current, which results from changes in common-mode voltage and presents major difficulties for transformerless PV integration.

A basic analysis of the traditional full-bridge inverter topology, including its operation under bipolar and unipolar PWM schemes, was conducted at the start of the study. This was used as a point of reference to emphasize the benefits and drawbacks of transformerless substitutes.

A detailed examination of the HERIC inverter demonstrated that it successfully reduces common-mode voltage fluctuations because of its unique freewheeling paths. Similarly, the H5 inverter, including an upgraded version, was investigated in detail, paying special attention to the effect of junction capacitance during switching transitions, which is frequently overlooked in simplified models.

The thesis investigated both inverters' reactive power capabilities in addition to their ability to suppress leakage current. In order to improve compliance with contemporary grid standards like IEEE 1547, a modulation technique was put forth that would allow reactive power injection in non-unity power factor situations. The effectiveness of the suggested strategy in improving inverter functionality without sacrificing performance or raising leakage currents was confirmed by simulation results.

In conclusion, the comparative analysis demonstrates that in transformerless PV applications, both the HERIC and H5 topologies provide notable benefits over conventional full-bridge designs. Future solar energy applications will benefit from safer, more effective, and grid-compliant inverter systems thanks to the knowledge gathered from this study.

This study presented an in-depth analysis of the HERIC and H5 transformerless inverter topologies in photovoltaic grid-connected systems; however, plenty of opportunities for future research remain. First, the effect of real-world grid disturbances, like voltage sags and frequency deviations, could be studied to examine inverter robustness under dynamic conditions. Furthermore, testing the results with a hardware prototype would make the simulation-based findings stronger and give us a better idea of the problems that could come up when putting them into practice.

Future research may investigate the incorporation of sophisticated control algorithms, including model predictive control or AI-driven optimization, to further diminish leakage current and improve dynamic performance. Finally, the suggested way to control reactive power could be expanded to include features like voltage regulation, fault ride-through, and grid-forming operation in microgrid situations.

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