POLITECNICO
MILANO 1863

SCUOLA DI INGEGNERIA INDUSTRIALE
E DELL'INFORMAZIONE

Analog-Digital CMOS Controller for Real Time Reconfiguration of Integrated Photonic Circuits

Tesi di Laurea Magistrale in
Electronics Engineering - Ingegneria Elettronica

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Academic Year: 2021-22

Abstract

Silicon Photonics is the technology that allows to integrate complex optical circuits, such as telecommunication routers, on a silicon wafer, adopting the same fabrication steps of the well known and long established CMOS process. One of the main obstacles to the actual application of this solution is the high sensitivity of optical devices on temperature variations and process tolerances, which may impair their functionality up to the point of making them unusable as stand-alone architectures. It is thus necessary to supply the photonic integrated circuit (PIC) with a closed-loop electronic control system that stabilizes the working point of the PIC and eventually adds some reconfigurability to it. The integrated nature of the photonic circuit suggests that this dedicated electronics should be realized as an ASIC as well, taking full advantage of the compactness, speed and limited power dissipation allowed by the CMOS integration process.

A mixed-signal architecture aimed to the stabilization and reconfiguration of a matrix (mesh) of Mach-Zehnder Interferometers (MZI) is proposed in this thesis. It is a structure of particular interest because it allows to implement several linear optical transfer functions, with applications ranging from signal routing and multiplexing to free-space optics.

First, the optical response of the device is studied in detail, and an integral control strategy based on the dithering technique, which allows to lock the MZI either to a minimum or a maximum of its transfer function thanks to the extraction of its first derivative (with respect to the phase shift induced by thermal actuators), is defined. An estimation of the closed-loop bandwidth of the system is also provided, demonstrating that it can compensate input phase disturbances in the kHz range.

In the following, the design of a front-end analog stage for the acquisition of the signal from the photodetectors (photodiodes) is shown, with focus on the issues related to the wide range of input currents to be managed, the limited resolution of the ADC and noise, and how they were solved.

Finally, the bold improvement in terms of bandwidth, speed, integration density and reconfigurability of the PIC with respect to previous, fully-analog architectures is shown

thanks to the massive introduction of digital electronics in the system. Despite the relatively large feature size of the technology adopted for the design (AMS C35B4), it is proved that the system can work on a 8-inputs MZI diagonal mesh, a complexity that can easily be increased thanks to the modularity of the electronic system.

Keywords: Electronics, Silicon Photonics, Mach-Zehnder Interferometer, Closed-Loop Control, Analog-Digital, CMOS, Integrated Circuit, Mixed-Signal.

Abstract in lingua italiana

La fotonica su silicio è la tecnologia che permette di integrare su wafer dei circuiti ottici complessi, quali ad esempio router per le telecomunicazioni, utilizzando metodi di fabbricazione che la tecnologia CMOS ha reso disponibili ormai da anni per l'elettronica integrata. Uno dei principali ostacoli all'effettivo utilizzo di questa soluzione è l'elevata sensibilità dei dispositivi ottici alle variazioni di temperatura e alle tolleranze del processo, che possono rivelarsi tali da impedire il funzionamento autonomo e indipendente del sistema. Si rende pertanto necessario il controllo in anello chiuso del circuito fotonico per stabilizzare il punto di lavoro dei dispositivi, ed eventualmente aggiungere la possibilità di riconfigurare a piacere lo stesso. La natura integrata del sistema ottico lascia intuire che pure l'elettronica possa e debba essere realizzata in tecnologia CMOS sotto forma di ASIC, in modo da sfruttare tutti i vantaggi che ne derivano in termini di compattezza, velocità e dissipazione di potenza.

In questa tesi viene proposta un'architettura mixed-signal avente lo scopo di stabilizzare e riconfigurare il punto di lavoro di una matrice (*mesh*) di interferometri Mach-Zehnder. La struttura risulta di particolare interesse in quanto consente di implementare svariate funzioni di trasferimento ottico lineari, con possibili applicazioni che spaziano dal *routing* e il *multiplexing* di segnali all'ottica *free-space*.

Innanzitutto viene studiata in dettaglio la risposta del dispositivo ottico, e viene definita una strategia di controllo di tipo integrale basata sulla tecnica di *dithering*, che permette di fissare il punto di lavoro dell'interferometro intorno a un minimo (o massimo) della sua funzione di trasferimento attraverso l'estrazione della derivata prima della stessa rispetto allo sfasamento indotto dagli attuatori termici. Viene anche fornita una stima della banda del sistema in anello chiuso, che dimostra la capacità dello stesso di compensare disturbi in ingresso fino a frequenze di qualche kHz.

Successivamente, si propone in dettaglio l'architettura del front-end analogico con cui acquisire il segnale ottico, rilevato attraverso dei fotodiodi. Particolare attenzione è rivolta all'ampio intervallo del segnale di corrente da convertire, alla limitata risoluzione dell'ADC e al rumore, e si dimostra come questi problemi siano stati risolti.

Infine, viene mostrato il significativo miglioramento, rispetto a soluzioni completamente analogiche, in termini di banda, velocità, densità d'integrazione e riconfigurabilità del circuito ottico reso possibile dalla massiccia introduzione dell'elettronica digitale nell'anello di controllo. Nonostante il nodo tecnologico relativamente ingombrante della tecnologia adottata (AMS C35B4), si prova che il sistema può essere usato in una mesh diagonale con 8 ingressi. La modularità che caratterizza il sistema consentirà di utilizzarlo, opportunamente replicato, per il controllo di circuiti ottici ancora più complessi.

Parole chiave: Elettronico, Fotonica su Silicio, Interferometro Mach-Zehnder, Controllo in Anello Chiuso, Analogico-Digitale, Mixed-Signal, Circuito Integrato, CMOS.

Contents

1 | Introduction

1.1. Why Photonics?

The past 70 years have been characterized by a constant improvement of the fabrication process of electronic devices, resulting in an ever growing complexity, density and speed of integrated circuits (IC). As more and more devices are fitted into the same silicon area, a problem arises with metal connections: bandwidth is always traded against power dissipation, integration density against sensitivity to cross-talk and external disturbances. It can be shown that the information-carrying capacity of a wire of cross-section A and length L is proportional to A/L^2 [1]: while this might not be an issue for wires inside the chip, the scaling that would be needed for global, core-to-core and core-to-memory interconnections becomes just unfeasible, whereas the number of repeaters to be placed along the line would lead to unacceptable power dissipation and area occupation [2]. All these issues suggest to look for a completely different, "more-than-Moore" solution to carry information and even to implement matrices for signal processing: light. Unlike electrons, photons do not have rest mass nor charge, which makes them immune to whatever interference.

Optical connections already represent the gold standard for long-range data transmission, with older technologies like coaxial cables being progressively replaced by optical fiber. In recent years, in response to the issues described above, photonic solutions have been proposed also for short and ultra-short distances. As of today, light-enabled products and services are worth an estimated $7 to $11 trillion, accounting roughly for 11% of world's GDP, whereas core photonic components revenues showed a steady annual growth rate of 7.6% in the last 10 years, and are expected to reach $378 billion by the end of 2022 [3].

A key factor in determining the success of a given technology is the possibility to integrate its devices and to exploit already existing fabrication processes. The fact that optical properties matter as much as electrical ones has led to the implementation of many different solutions, each one with its pros and cons, including silicon nitride, indium phosphide, lithium niobate and, obviously, silicon. In particular, CMOS Integrated Silicon Photonics is a promising candidate for the realization of optical interconnections,

even inside the chip. The possibility to exploit the long-established CMOS technology paved the way for the realization of complex yet relatively cheap photonic circuits, up to the point of building fully-optical integrated elaboration systems, such as ROADM (*Reconfigurable Optical Add-Drop Multiplexer*) [4].

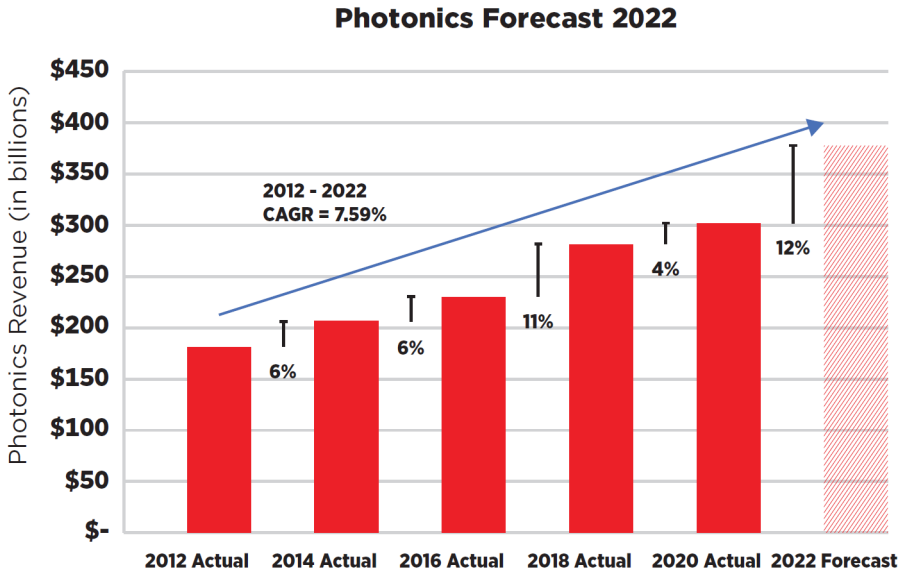


Figure 1.1: Photonic components global revenues by year [3]

1.2. Silicon Photonics

In addition to the advantages related to cost and simplicity of the CMOS fabrication process, silicon also offers some excellent optical properties in the NIR (*near-infrared*) wavelength range.

First of all, the SOI (*Silicon On Insulator*) technology allows to combine two materials, Si and its oxide (SiO_2), whose refractive indexes are, respectively, $n_{Si} \approx 3.45$ and $n_{SiO_2} \approx 1.45$. With a resulting index contrast of $\Delta = \frac{n_{Si}-n_{SiO_2}}{n_{Si}} \approx 0.6$, SOI makes possible to build waveguides confining light within a section that can be as small as $0.1\mu m^2$. Second, silicon is almost transparent at MIR wavelengths, with the losses, mainly due to scattering events at the Si/SiO_2 interface, in the order of 1-3 dB/cm for $\lambda = 1300$nm and $\lambda = 1550$nm, i.e. the two wavelengths typically employed in optical communications: it is indeed an acceptable value for short range (<1cm) communications, a good compromise between integration density and attenuation. It is worth mentioning that the energy of a single NIR photon (0.8-1eV) is not sufficient to overcome the energy gap between valence and conduction band of a Si crystal (1.12eV at 300K): without any imperfection at Si/SiO_2

interface, silicon would be perfectly transparent at the wavelengths of interest.

1.2.1. Waveguides

Waveguides are the building blocks of every photonic system, as they are the devices that carry the optical signal around the system. Despite several architectures and design solutions having been proposed (Fig. 1.3), they all rely on the same fundamental concept: that a central silicon core, typically lightly p-doped, has a higher refractive index than the surrounding cladding (made of SiO_2 in the case of SOI), thus allowing for total reflection and in conclusion for light confinement. It is also possible to build bent waveguides: unsurprisingly, radiation losses increase for tighter bending radius and decrease for higher index contrast (Fig. 1.2). It is now useful to introduce a concept that will come into help later on: the *optical length* of a silicon waveguide of length L is defined as

$$L_{opt} = n_{Si} \cdot L \tag{1.1}$$

A wave with wavelength λ entering with an initial phase ϕ_0 will accumulate an additional phase shift

$$\Delta\phi = \frac{2\pi}{\lambda} L_{opt} \tag{1.2}$$

With a very simplified notation, the relation between input and output transverse components of the electric field can be written as

$$E_{out} = E_{in} \cdot e^{-j\Delta\phi} = E_{in} \cdot e^{-j\frac{2\pi}{\lambda}L_{opt}} \cdot e^{-\frac{\alpha L}{2}}, \tag{1.3}$$

with α being the power losses per unit length.

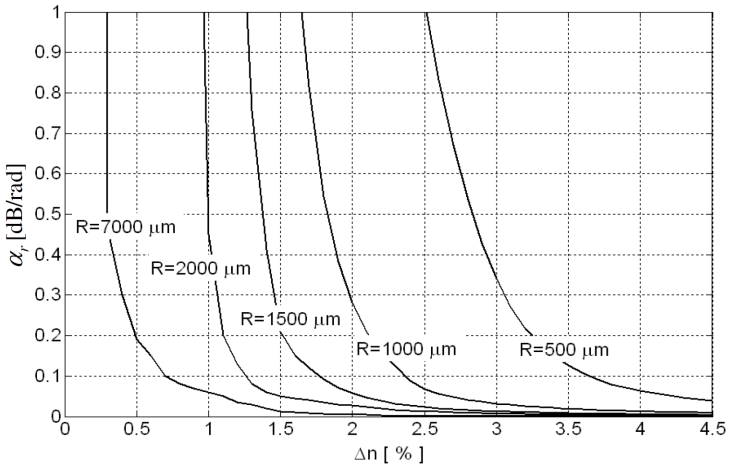
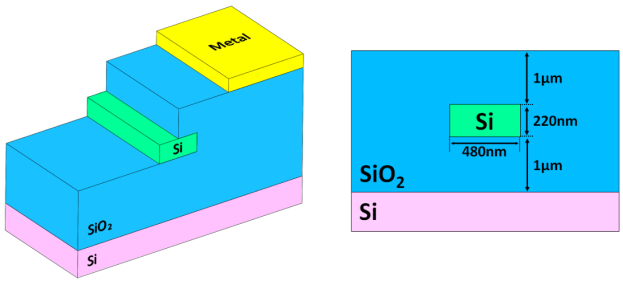
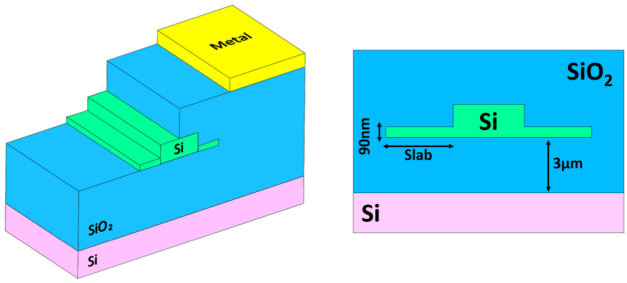


Figure 1.2: Radiation losses vs index contrast Δn and bending radius R [5]



(a)



(b)

Figure 1.3: Two typical architectures for waveguides: *buried* (a) and *rib* (b)

1.2.2. Directional Couplers

To implement more complex functionalities than a simple phase shift, a photonic device capable of transferring optical power from one waveguide to another is needed. The structure that performs this task is the *directional coupler*. Unlike metal waveguides, where the propagation modes are perfectly confined within the core, in dielectric ones an evanescent field is present also in the cladding: when two waveguides are sufficiently close, their fundamental modes are coupled and power exchange becomes possible. In the simplified assumption of a synchronous coupler, i.e. a device whose waveguides have identical fundamental modes, the 2x2 matrix describing the transfer function of the component can be written as:

$$T_C = \begin{bmatrix} \cos(kL) & -j\sin(kL) \\ -j\sin(kL) & \cos(kL) \end{bmatrix} \tag{1.4}$$

L is the length of the coupler, while k is a parameter descending from the physical design variables, such as the shape and the distance between the waveguides and even, although with very weak dependence, on the wavelength. It is important to observe that in a synchronous coupler full power transfer is possible from one waveguide to another (when $kL = \frac{\pi}{2} + N\pi$). In addition to that, no matter the fraction of transferred power, the -j

factor in the non-diagonal elements of the matrix shows that the wave "jumping" from one branch to the other is phase shifted by $-\frac{\pi}{2}$. A particular yet very common case is the so-called *-3dB coupler*, where light is equally shared between the two waveguides. It can be obtained with $kL = \frac{\pi}{4}$, resulting in:

$$T_C = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -j \\ -j & 1 \end{bmatrix} \tag{1.5}$$

As a final remark, when two coherent waves enter the component, the coupling effect allows interference between the waves that end up in the same branch and output power will be partitioned accordingly to their relative initial phase shift. The possibility to act on this shift is the key to programmable optical circuits.

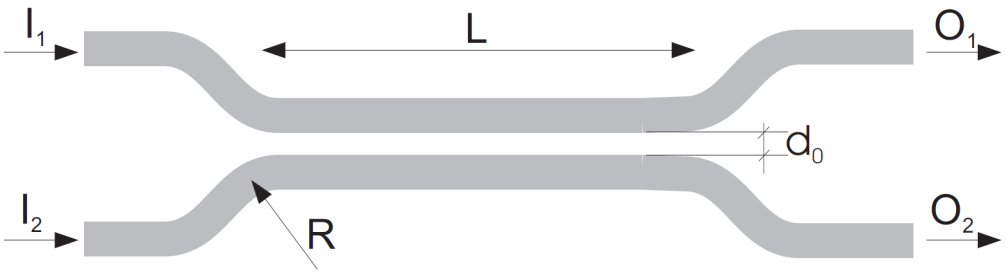


Figure 1.4: Scheme of a directional coupler

1.2.3. Mach-Zehnder Interferometers

It is possible to combine directional couplers and waveguides in order to create a more complex device: the *Mach-Zehnder Interferometer* (MZI). Despite it can be used also as a not-so-effective WDM (*Wavelength Division Multiplexing*) filter, in this project MZIs are used in order to completely steer the optical power towards a single output, independently from the wavelength (provided that the two input waves are coherent, of course). As portrayed in Fig. 1.5, a MZI is the series of two directional couplers, providing beam splitting and recombination, connected by two waveguides in between, introducing phase shift. The matrix describing this phase shifting behaviour can be written as:

$$T_{WG} = \begin{bmatrix} e^{-j\phi_1} & 0 \\ 0 & e^{-j\phi_2} \end{bmatrix} \tag{1.6}$$

where we recall that $\phi = L_{opt}\frac{2\pi}{\lambda}$.

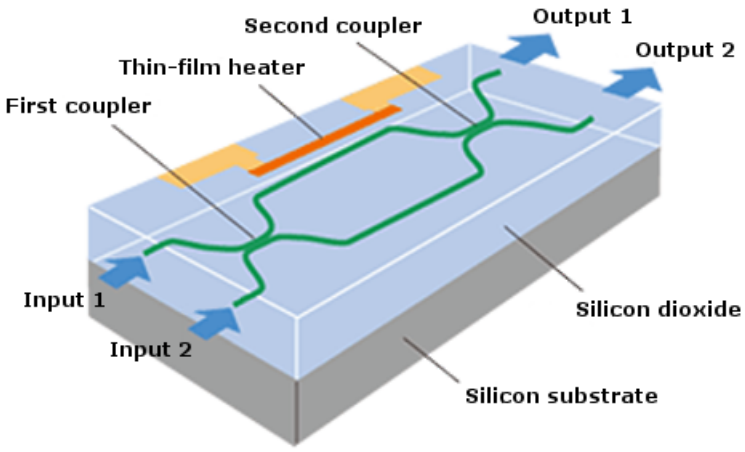


Figure 1.5: Schematic representation of a MZI working as an optical deviator [6]

From 1.4 it follows that the transfer matrix of a MZI, for what concerns the transverse components of the electric fields and assuming identical direction couplers, can be written as:

$$\begin{bmatrix} E_{out1} \\ E_{out2} \end{bmatrix} = T_c \cdot T_{WG} \cdot T_c \begin{bmatrix} E_{in1} \\ E_{in2} \end{bmatrix} \tag{1.7}$$

Finally, considering $\Delta\phi = \phi_1 - \phi_2 = \frac{2\pi}{\lambda}\Delta L_{opt}$, assuming that the two waves are in phase when entering the MZI and using -3dB couplers (i.e. with $kL{=}\frac{\pi}{4}$), the output power distribution can be easily written as

$$P_{out,1} = \sin^2(\frac{\Delta\phi}{2}) \text{ and } P_{out,2} = \cos^2(\frac{\Delta\phi}{2}) \tag{1.8}$$

It is possible to combine more interferometers in a so-called *mesh*, implementing larger, more complicated and, as it will be shown in the following, reconfigurable matrices.

1.2.4. Thermal actuators

Recalling 1.1, 1.2 and 1.8, a question may arise around the possibility of modifying $\Delta\phi$ in order to make the MZI programmable and suitable for operation in optical systems. Clearly, being the MZI an integrated device, it is not possible to modify its structural characteristics such as dimensions and shape; however, the refractive index of silicon is extremely sensitive to temperature variations (Fig. 1.6). On one side, this is a disadvantage, since an external control system is needed to stabilize the device: a 1K temperature variation may cause a shift in the optical response of an interferometer of 10GHz [7]. On the other side, the very same property is exploited in order to actively control the working

point of the MZI via a closed-loop electronic system.

The introduction of thermal actuators, called *heaters*, also depicted in Fig. 1.5, allows to locally modify the temperature and hence the refractive index of the waveguides: as a result, it is possible to modulate the relative phase shift between the two branches. Heaters are metal (usually Ti) resistors deposited on top of the SiO_2 cladding that surrounds the Si core, with a resistance value in the order of $R_H = 100 - 1000\Omega$. Each MZI typically has 2 heaters, on opposite sides, to adjust the relative phase shift before and after the directional couplers.

Temperature is adjusted by modifying the voltage drop across the component, i.e. the dissipated power. The maximum modulation speed is ultimately determined by the thermal time constant of the heaters, in the order of few µs: although there are more sophisticated techniques to realize a much faster phase modulation, in the order of 10-100GHz [8], with a very simple architecture heaters are suitable for modulation in the order of some kHz, allowing to implement complex control strategies.

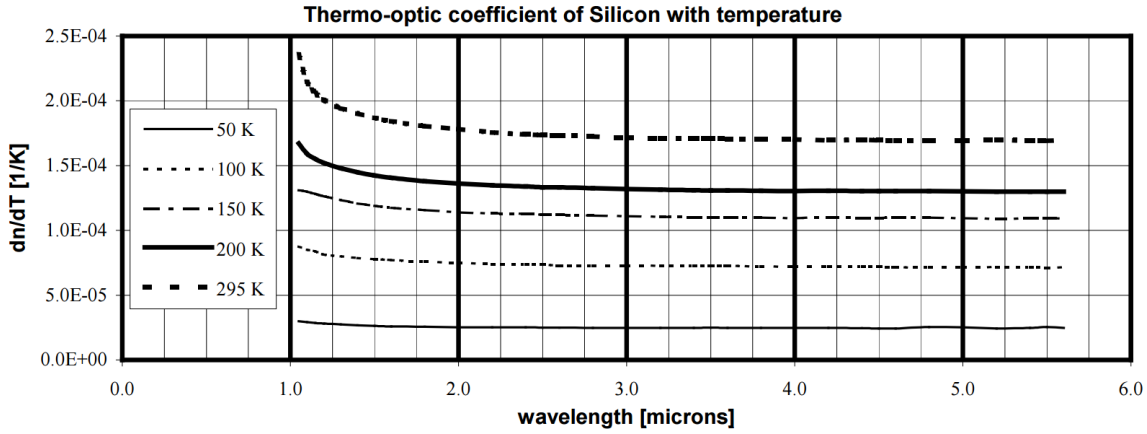


Figure 1.6: Silicon refractive index sensitivity on temperature for different wavelengths

1.3. The need for control electronic

The discussion made in Sec. 1.2 should have made clear enough one thing: that no photonic integrated circuit realized in Silicon Photonics technology could work as a stand-alone, independent system: thermal drifts and process-related imperfections would impair the operations at the point of making the whole optical device unusable. What is needed is thus a closed-loop control system able to stabilize the working point of each device of the PIC, and eventually to steer it towards an arbitrary reference value.

It is needless to state that such control loop, which is also comprehensive of the optical

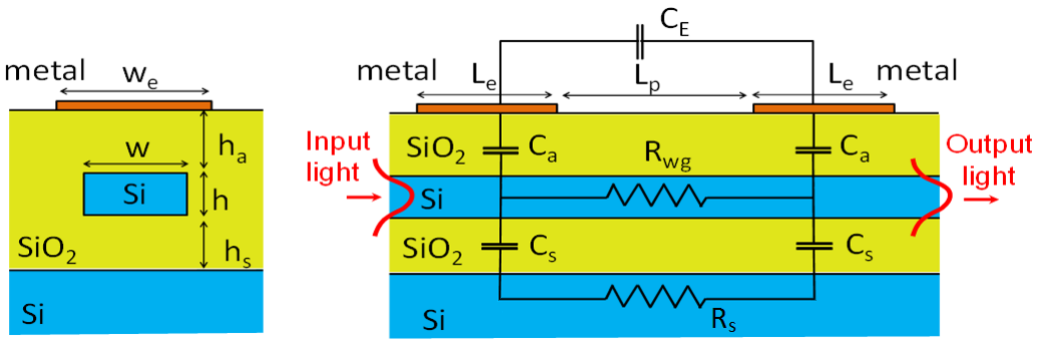


Figure 1.7: Electrical model of the CLIPP sensor

device, should be an electronic one. It is more interesting to observe that, whereas many effective solutions have already been proposed to this scope adopting discrete components, the integrated nature of Silicon Photonics suggests that the optimal and ultimate architecture for the control system should be that of an ASIC. The advantages coming with this solution would be two sided: in parallel to those typical of whatever integrated circuit (compactness and scalability, speed, low power consumption), the possibility of using the CMOS technology for both the photonic and the electronic part suggests that the two could be integrated on the same silicon wafer, thus paving the way to "mixed-signal" circuits where both photons and electrons are exploited to implement the functionalities for which they are respectively more suitable.

1.3.1. Sensors

The optical device is indeed a part of the closed loop described above: the electronic controller should be able both to extract information about its state and to drive the actuators that control the phase shift induced in the waveguides. There are two ways of sensing light, each one with its pros and cons: either with transparent detectors or with invasive ones.

Transparent detectors - CLIPP

One clever way to sense the amount of optical power circulating in the waveguides is to exploit the very little losses of infrared light in silicon, that would be in any case present in the waveguides[1]. This is the working principle of the CLIPP sensor [9], schematically portrayed in Fig. 1.7: the circuit is capacitively coupled to the waveguide and senses, with a lock-in technique, the conductivity variations of the crystal associated with photons

[1]Losses are due to defects at the Si-SiO_2 interface. It is somehow curious that the CLIPP would be ineffective if the waveguide could be a perfect, defects-free silicon crystal.

absorptions to determine the amount of light. The advantage is pretty clear: that the sensor is non-invasive, and no optical power has to be "wasted" to provide the necessary information to the control-loop: it is possible to build a *NxN* optical matrix, where no output is "blocked" by a sensor. There are, however, also a number of disadvantages, the most notable of which is that, due to the silicon transparency for NIR wavelengths, the signal to be detected is very weak and a lot of effort in terms of power dissipation and area occupation has to be put in the design of the analog stage of the ASIC.

Photodiodes

The very same dissertation made for the CLIPP can be reverted, in terms of pros and cons, for what concerns an invasive type of detectors, like photodiodes. It is clear that placing a photodiode on one of the two outputs of the MZI is equivalent to completely block the wave travelling in that branch of the device. As a result, the number of optical linear transfer functions that the **mesh** can implement is reduced with respect to the case of transparent detectors. It is also true, however, that the photodiode, which is not made of silicon (the choice in this project fell on a Ge-based integrated photodiode), allows for a complete absorption of the photons travelling inside the waveguide: the consequence is an improved sensitivity, that will allow for a more precise control of the devices and a more sustainable trade-off between power dissipation, occupied area and signal-to-noise ratio of the ASIC, allowing for the implementation of some interesting photonic circuits, like the one shown just below.

1.3.2. A possible application for a MZI mesh: Self-Aligning Universal Beam Coupler

An actual application in free space optics of the circuit portrayed in Fig. 1.8 is the self-aligning beam coupler [10].

The photodetectors sense light intensity in the waveguides, which is used as a state variable for the closed-loop system that drives the actuators, eventually closing the loop on the optical device. The three interferometers are sequentially regulated in order to steer all the optical power collected at the input towards just one output (OUT_1). This is the same as saying that the MZIs progressively compensate ("aligns") the phase shift between the waves travelling in the mesh, so as to always deliver a constructive interference that eventually collimates the light into a single output waveguide.

Such circuit can be used in order to establish perfectly aligned bidirectional optical communication channels [11]. In fact, when light is injected into the output (red wave), it

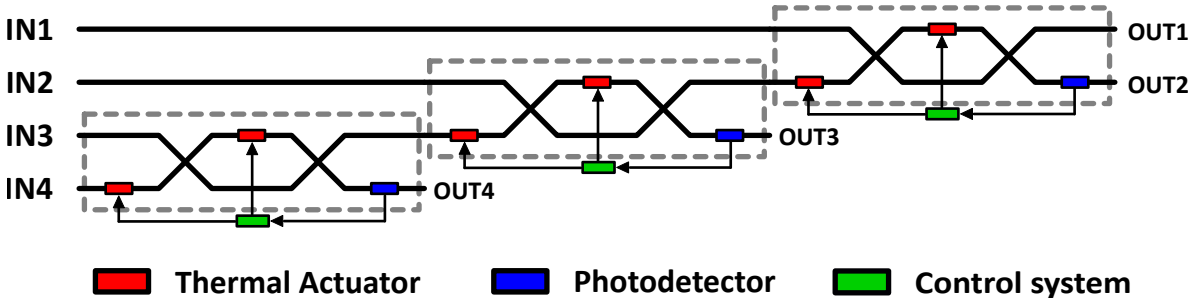


Figure 1.8: Scheme of a self-aligning universal beam coupler

undergoes the opposite operations with respect to the optical beam injected at the input side (orange wave). If the inward propagating waves (orange in Fig. 1.9) have their relative phase shift cancelled when passing through the component, a backward propagating wave injected at output (red) will accumulate a phase shift that will reproduce the same exact pattern when emitted at input side. This is equivalent to say that, if the inward wave were to be reflected back into the device at the output, the resulting backward wave would be projected onto the source were the beam first originated.

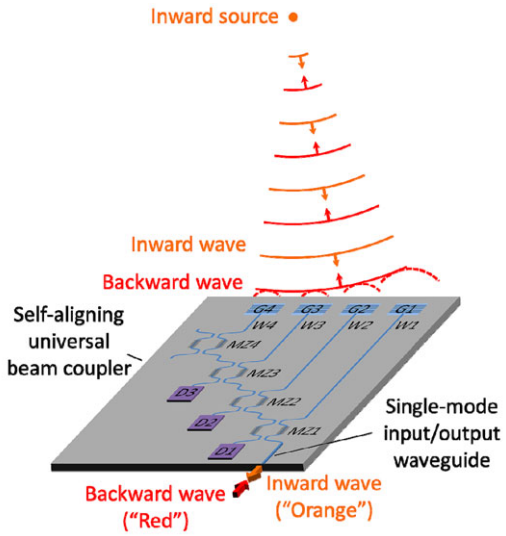


Figure 1.9: A mesh of MZIs implementing a 4 channels self-aligning universal beam coupler [11]

Furthermore, the power dissipated by the heater, which is related to the applied control voltage V as $P_{DISS} = \frac{V_H^2}{R_H}$, can be monitored in order to determine the induced phase shifts, which obviously corresponds to the delays existing between the waves at the input, and reconstruct the profile of the wavefront propagating into free-space.

2 | Control System

Introduction

Developing an electronic control system is of the utmost importance to let complex photonic circuits work properly. As highlighted in Chapter 1, without a feedback control system able to monitor and fix the working point of the device, thermal drifts, parasitic effects and process related defects would affect the operation and undermine, for example, the filtering capability of the interferometric device. Most control systems are now implemented by means of discrete components. Although they proved to be effective in the regulation of the optical circuit, they do not take advantage at all of the integrated nature of PICs (*Photonic Integrated Circuits)*: since the mesh of MZIs is created on a silicon wafer, with the very same fabrication steps adopted for electronic circuits, it is intuitive that the control system could be realized with an ASIC as well. This solution becomes a preferred one as PICs increase in number of devices and complexity: it is fundamental that the dedicated control electronics has a comparable size to that of the interferometer, in the order of few mm^2. This is also one of the main motivations behind the adoption of a mixed-signal solution: the digital part of the circuit, that will be treated in Chapter 4, could be scaled by moving to a smaller process node with respect to the 0.35 μm. Halving the feature size would allow a factor 4 improvement in system integration density.

The advantages coming with the monolithic integration of the electronic control system, namely the reduced area occupation and increased complexity, as well as the limited power dissipation, are paid with poorer reconfigurability, despite some parameters could still be adjustable at digital level (see Chapter 4). Hence the necessity to have a deep understanding of the photonic devices presented in Chapter 1, with particular focus on their response to the variation of the control voltage on the thermal actuators, and the associated non-linearity, for which a solution will be proposed.

The control algorithm is based on the dithering technique: measuring the derivative of the transfer function of the MZI, instead of trying to determine its absolute value, helps getting rid of any offset affecting the optical device, and through the information carried

by the sign of the derivative it is possible to infer the direction to be taken to steer to system towards a maximum or a minimum.

Finally, an analytical computation of the loop gain and the associated bandwidth is presented, as well as a solution for implementing a tunable bandwidth.

2.1. Optical system response

Eq. 1.7 already showed that the output electric field of each branch of the MZI is associated to the phase shifts $\Delta\phi_{1,2}$ induced on the mode propagating inside the waveguides. With no lack of generality, the overall transfer function of the MZI, connecting input and output electrical field, can be written as the product of the matrices describing its 4 building blocks (2 heaters and 2 couplers):

$$\begin{bmatrix} E_{OUT1} \\ E_{OUT2} \end{bmatrix} = T_{MZI} \cdot \begin{bmatrix} E_{IN1} \\ E_{IN2} \end{bmatrix} \tag{2.1}$$

$$T_{MZI} = \begin{bmatrix} cos(kL) & -jsin(kL) \\ -jsin(kL) & cos(kL) \end{bmatrix} \cdot \begin{bmatrix} e^{-j\phi_{H2}} & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} cos(kL) & -jsin(kL) \\ -jsin(kL) & cos(kL) \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ 0 & e^{-j\phi_{H1}} \end{bmatrix}$$

Output field (and power) distribution depends on the initial phase shift and intensity of input fields, on the partition operated by the couplers and on the phase shift ϕ_1, ϕ_2 induced in the waveguides by the heaters.

The contributions from the directional couplers are fixed: they always introduce a $\frac{\pi}{2}$ phase shift on the *cross* port, and their parameter kL only depends on the process. Still, it is possible to act on the heaters to modify the phase shift induced in the waveguides before

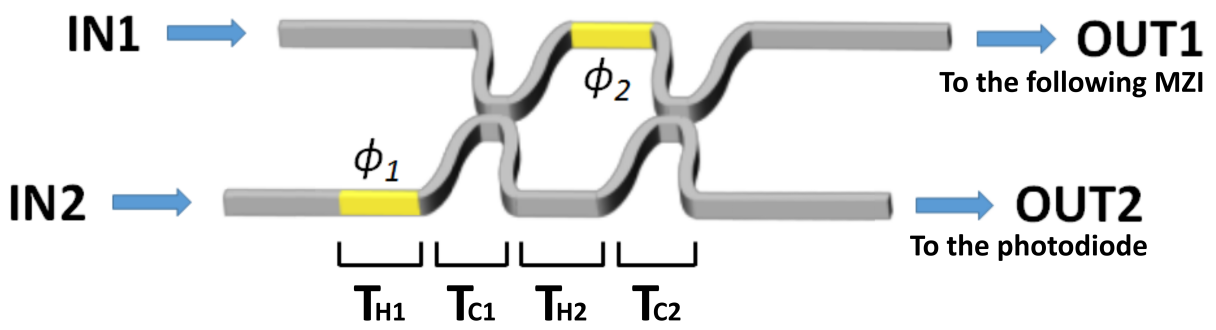


Figure 2.1: Model of a Mach-Zehnder interferometer where the contributions from heaters (T_H, yellow) and couplers (T_C) are highlighted

the first directional coupler and between the two.

Fig. 1.6 shows that, around 300 K, the refractive index of silicon is modified by $\Delta n \approx 1.8 \cdot 10^{-4}$ by a 1 K temperature variation: considering a wavelength λ_0=1550 nm, it means that over a distance $L = \frac{\lambda_0}{\Delta n} \approx 9$ mm the propagating wave accumulates an extra 2π delay every 1 K temperature increase.

It might be useful to plot the output power on one branch, written as $P_{OUT1} = |E_{OUT1}|^2$, as a function of device (kL, ϕ_1, ϕ_2) and input ($P_{IN1,2}$, $\phi_{IN1,2}$) parameters. Fig. 2.2 shows that an unbalance in kL (with respect to the *-3 dB coupler* case, i.e. kL=$\frac{\pi}{4}$) or in the input power distribution distorts the map (Fig. 2.2b-c), whereas, as it could be easily expected, a variation of the initial phase operates a translation of the plot (Fig. 2.2d).

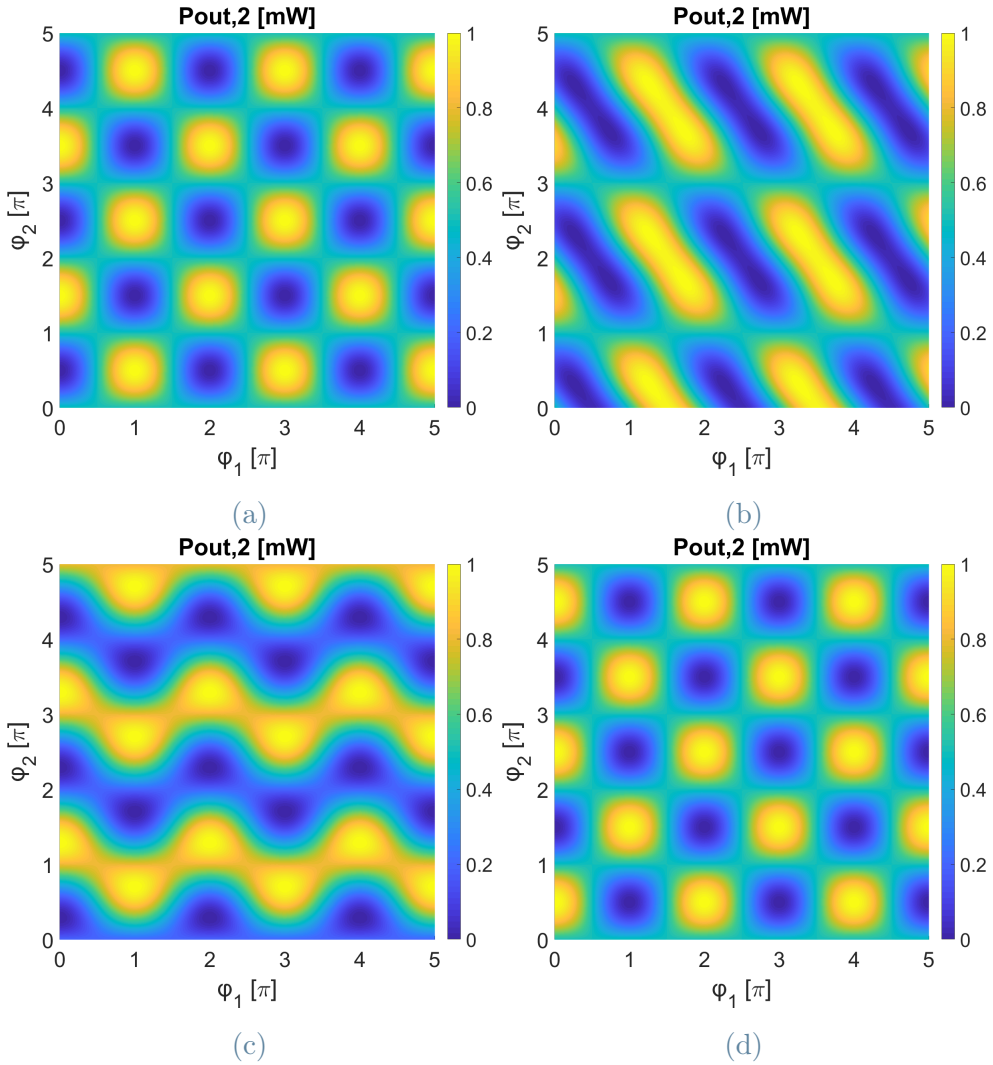


Figure 2.2: Mach-Zehnder interferometer maps. **(a)** $P_{IN1,2}$=0.5 mW, $\phi_{IN1,2}$=0, kL=$\frac{\pi}{4}$; **(b)** $P_{IN1,2}$=0.5 mW, $\phi_{IN1,2}$=0, kL=$\frac{\pi}{5}$; **(c)** P_{IN1}=0.2 mW, P_{IN2}=0.8 mW, $\phi_{IN1,2}$=0, kL=$\frac{\pi}{4}$; **(d)** $P_{IN1,2}$=0.5 mW, $\phi_{IN1} = \pi$, $\phi_{IN2} = 0$, kL=$\frac{\pi}{4}$.

2.1.1. Optical system response in electric domain

To complete the analysis of the optical system, the response of the interferometer to the voltage V_H applied to the heaters should be studied. From the electrical standpoint, heaters are indeed resistors, integrated close to the waveguides, and dissipate a power $P_{TH}=\frac{V_H^2}{R_H}$. The local temperature is proportional to the dissipated power. By linearizing the plot of Fig. 1.6, it is possible to conclude that the induced phase shift is proportional to the dissipated power as well:

$$\phi_H \propto T_H \propto P_{TH} = \frac{V_H^2}{R_H} \tag{2.2}$$

It is thus possible to write a relation between the induced phase shift and the voltage V_H, which is the control variable of the system:

$$\phi_H = \phi_0 + \Delta\phi_H \cdot \frac{V_H^2}{V_{HMAX}^2} \tag{2.3}$$

V_{HMAX} being set to 6 V. The choice of an increased maximum voltage with respect to previous projects (5 V in [12]) is aimed to enlarge the span of phase shift covered by the heater. Fig. 2.3 shows the measured output current of a photodiode placed on one output of the MZI:

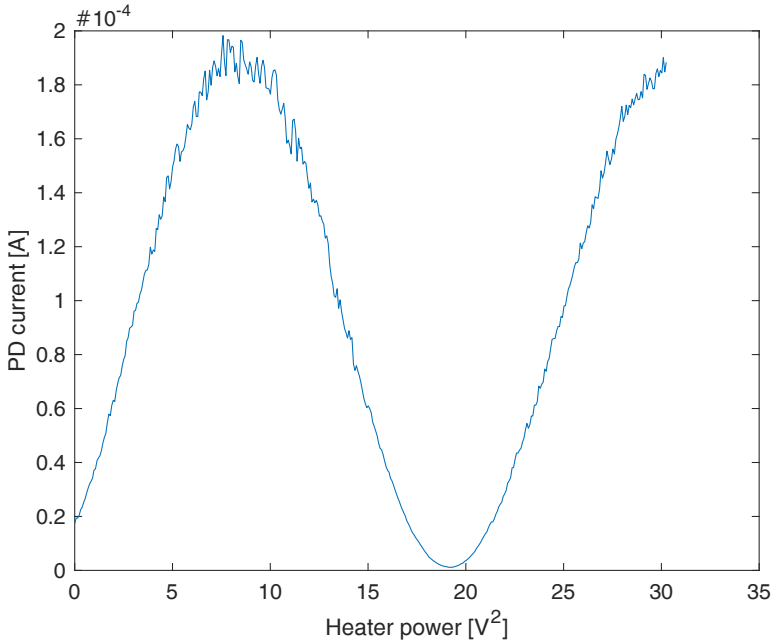


Figure 2.3: Measured output current on one MZI branch vs power dissipated by the heater

It is evident that, if V_{HMAX}=5 V, the heater dissipated power barely covers a 2π phase shift; furthermore, it is obvious that a fraction of the voltage range, close to 0 V and V_{HMAX}, should be excluded from the operating region and reserved for the activation of some reset mechanism to avoid system saturation. As a consequence, it is possible that either a minimum or a maximum of the transfer function cannot be reached with any valid value of V_H, thus suggesting that an increase in the voltage range might be appropriate. 6 V is a good compromise between the increased ϕ_H span and the absolute voltage ratings allowed by the technology used (AMS C35B4).

Whatever V_H, it is evident that a strong non-linearity is present: since $\phi_H \propto V_H^2$, the relation between control voltage variation ΔV_H and induced phase shift will be non-linear (quadratic) and dependent on the absolute value of V_H, something like:

$$\phi_H = \phi_0 + \Delta\phi_H \cdot \frac{(V_H + \Delta V_H)^2}{V_{HMAX}^2} = \phi_0 + \frac{\Delta\phi_H}{V_{HMAX}^2} \cdot (V_H^2 + \Delta V_H^2 + 2V_H\Delta V_H) \tag{2.4}$$

The effect is shown graphically in Fig. 2.4, plotting the output power of one branch of the MZI as a function of the control voltage of the heaters.

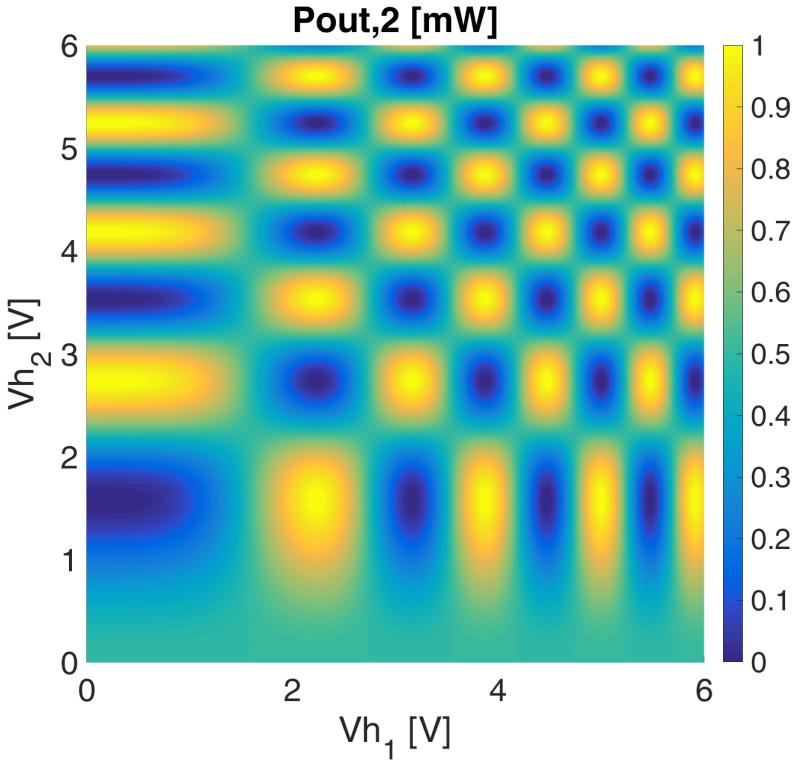


Figure 2.4: Electro-optical map of the Mach-Zehnder Interferometer, showing the distortion associated to the working point of the interferometer

2.1.2. Improving system linearity

The considered system is strongly non-linear: the quadratic relation between control voltage V_H and induced phase shift ϕ_H is only one among many. The most obvious and significant one is, of course, the sinusoidal transfer function from the power dissipated by the heater to the output current of the photodiode.

Despite many solutions having been proven to be effective even without any non-linearity adjustment [13], it might be interesting to try, at least, to contrast the quadratic dependence $\phi_H \propto V_H^2$. This is equivalent to saying that, denoting as C the control variable elaborated by the system, it should undergo a square-root operation, in order to have $V_H \propto \sqrt{C}$ and, as a result, $\phi_H \propto V_H^2 \propto C$.

Some examples are already present in literature, both digital ([14]) or analog ([15]. The solution proposed in this work is implemented inside the digital part of the ASIC dedicated to the control system, and consists of a very simplified yet effective approximation of the square root function by means of a series of straight lines with progressively reducing slope (Fig. 2.5).

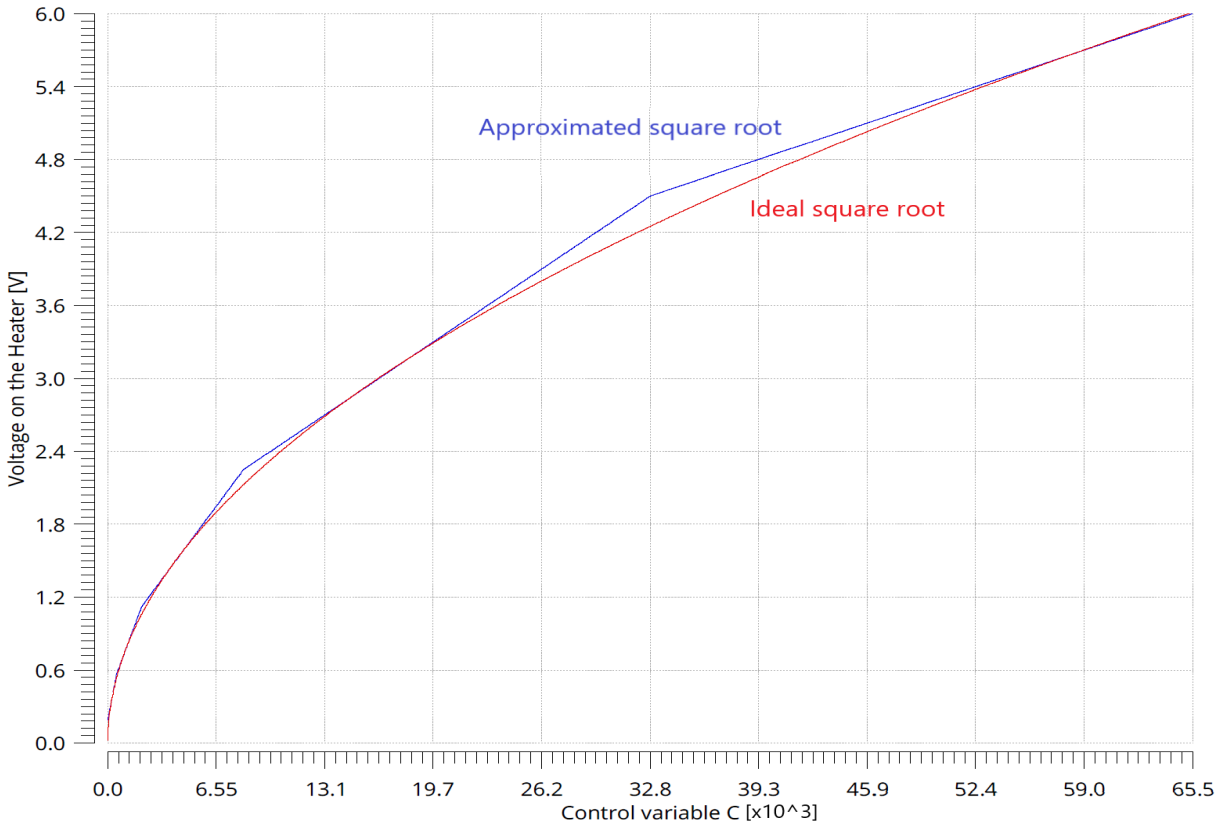
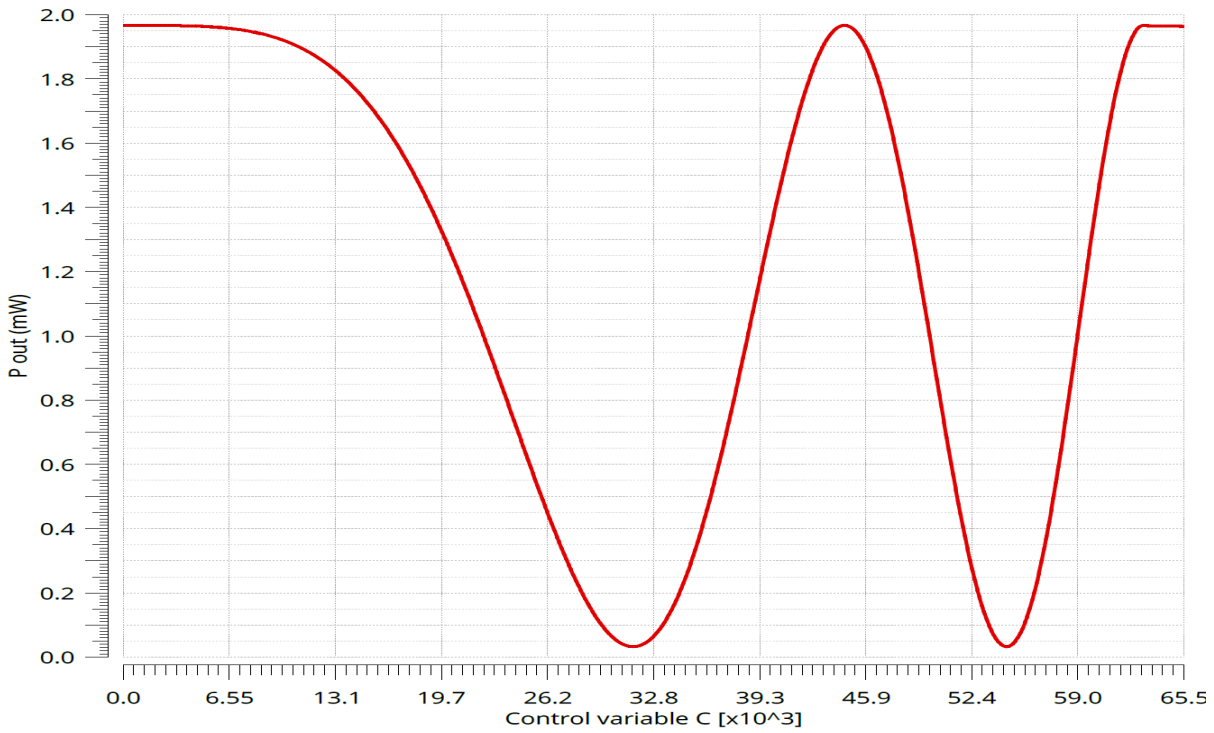
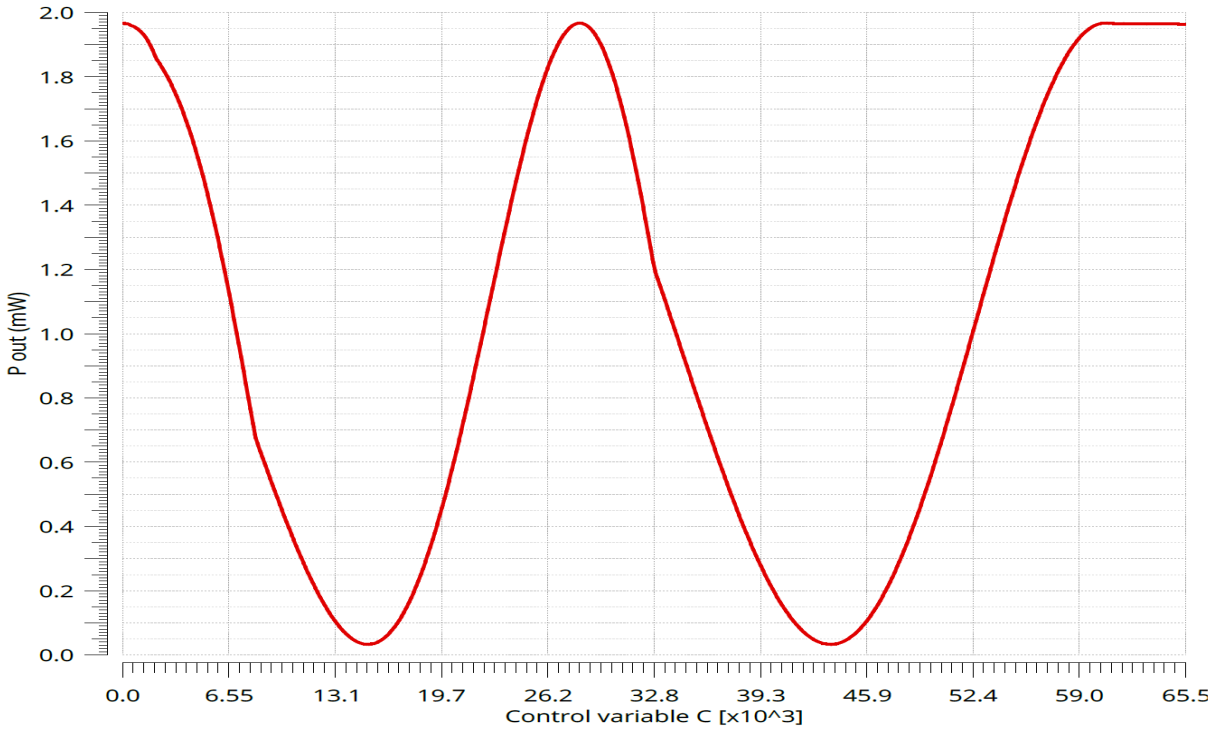


Figure 2.5: Comparison between a mathematical square-root of the control variable C and its approximated version. The output is normalized to 6 V.



(a)



(b)

Figure 2.6: Output power of the MZI as a function of the control variable C with (**a**) and without (**b**) making the square-root

.

The impact on the transfer function of the Mach-Zehnder has been simulated directly in the CAD environment used for the design of the integrated circuit (Cadénce Virtuoso), thanks to the Verilog-A models for the components of the optical system created in a previous work [16]. The digital block implementing the square root will be further analyzed in Chapter 4. By looking at the plots of Fig. 2.6, it is evident that, despite some distortion being introduced around the points where the slope of the approximated square root is modified, the overall effect is an improvement of the linearity of the system. The flattening of the transfer plot for large values of C is due to the saturation of the DAC connecting the digital block of the chip to the actuators.

2.2. Dithering-based control system

In most of the applications in Photonic Integrated Circuits, each interferometer of the mesh is supposed to fully steer the input optical power towards only one of the two outputs. By placing a sensor (a photodiode) on one output branch of each device, it is possible to extract all the information needed to implement a control loop that, acting independently on each heater, moves the MZI towards a minimum (or maximum) of its transfer function from whatever starting point. The fact that each device can be regulated without any influence from the other components of the mesh is crucial to increase the complexity of the optical circuit: the overall system will only have to be the replica of many control loops working in parallel.

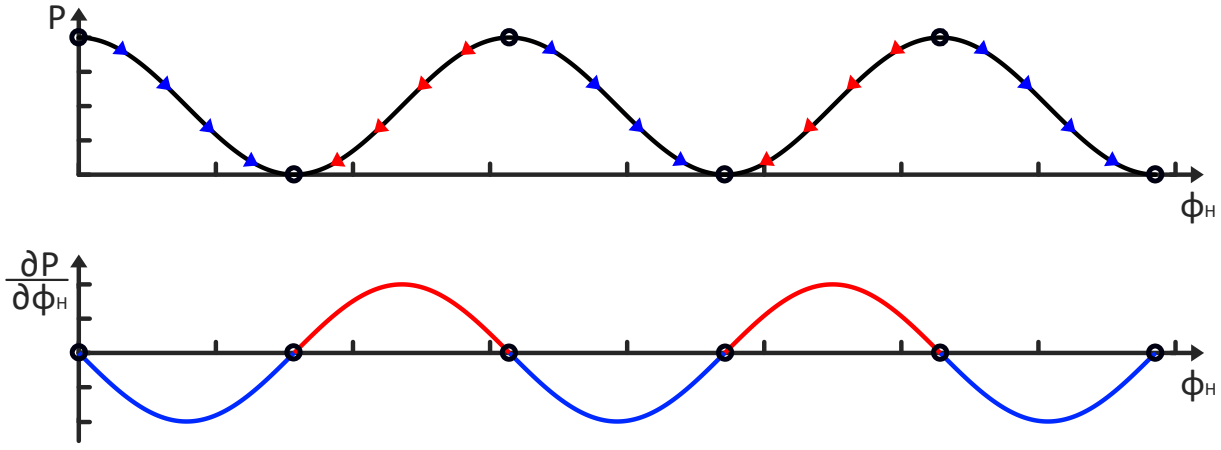


Figure 2.7: Output power and its derivative with respect to just one heater-induced phase shift

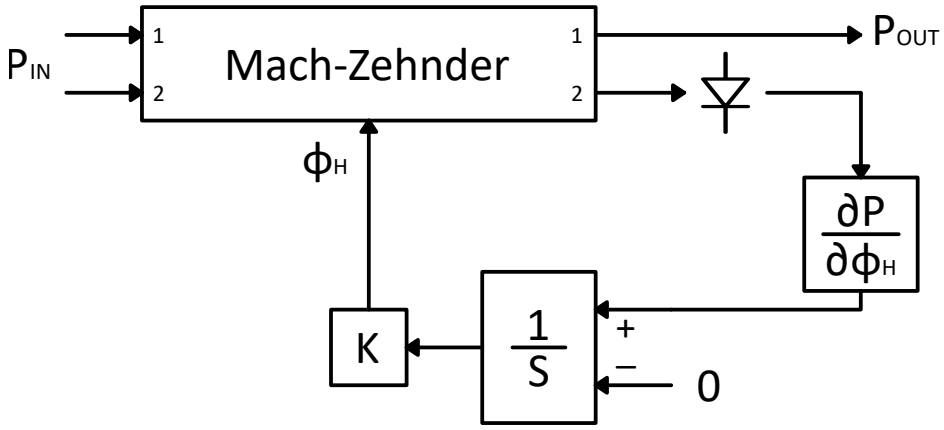


Figure 2.8: Simplified schematic of a single-variable integral control system

2.2.1. Single variable control system

Minimizing (maximizing) optical power in one branch means implementing a control system that drives the interferometer towards the minima (maxima) of its transfer function.

In an initial single-variable study, the voltage (as well as its induced phase shift) on one heater is considered fixed. With respect to the other heater phase shift, the output power $P_{OUT}(\phi_H)$ is a sinusoid (Fig. 2.7), whose parameters (amplitude, maximum and minimum value, initial phase) depends on both device (coupling coefficient) and input signal (power distribution, relative phase shift) related parameters.

Searching for such points is equivalent to search for the zeros of $\frac{\partial P_{OUT}(\phi_H)}{\partial \phi_H}$. In addition to that, differently from the primitive function, the derivative is not affected by any offset, meaning that its sign is indicative of which is the direction to be taken to lock the MZI on a minimum. As a consequence, it is natural to think of an integral control system that uses the information of $\frac{\partial P_{OUT}(\phi_H)}{\partial \phi_H}$ as the error signal. Multiplying the loop gain by -1, a very simple operation, allows to switch the target of the control loop from the maximum of the transfer function to the minimum and viceversa. In theory, it would also be possible to lock the device to whatever output power (actually, to a precise value of $\frac{\partial P_{OUT}(\phi_H)}{\partial \phi_H}$) by setting the proper reference signal at the summing node of the control loop (Fig. 2.8).

2.2.2. Two variables system

It is possible to extend the control strategy proposed in Sec. 2.2.1 to both heaters just by replicating the loop twice. Obviously there will be two control variables, corresponding to the powers dissipated by each heater, and two error signals, i.e. the partial derivatives of the MZI transfer functions (the ones shown in Fig. 2.2). The two loops work inde-

pendently, trying to bring to 0 their own partial derivatives, eventually locking again the device in a minimum/maximum of the transfer map (Fig. 2.9a).

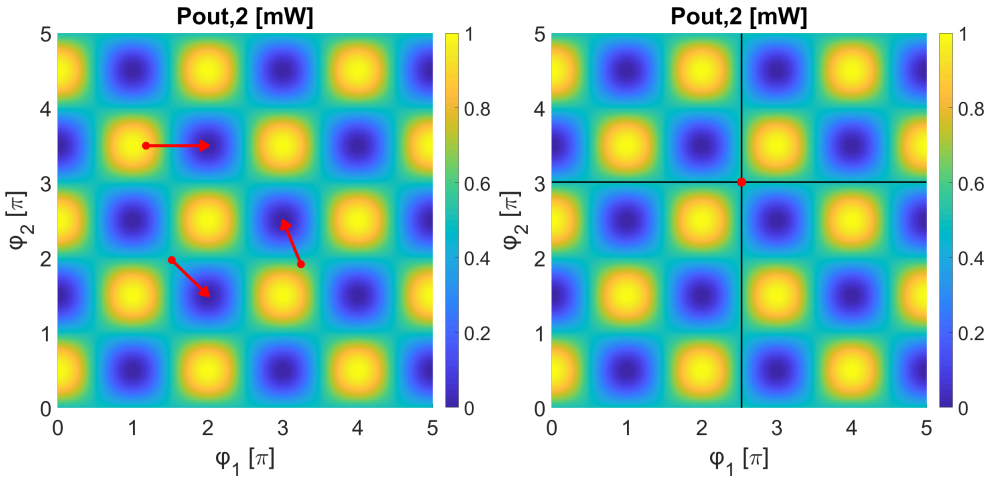


Figure 2.9: (**a**) Search for the minimum (maximum) in a 2 variables system; (**b**) example of unstable equilibrium point

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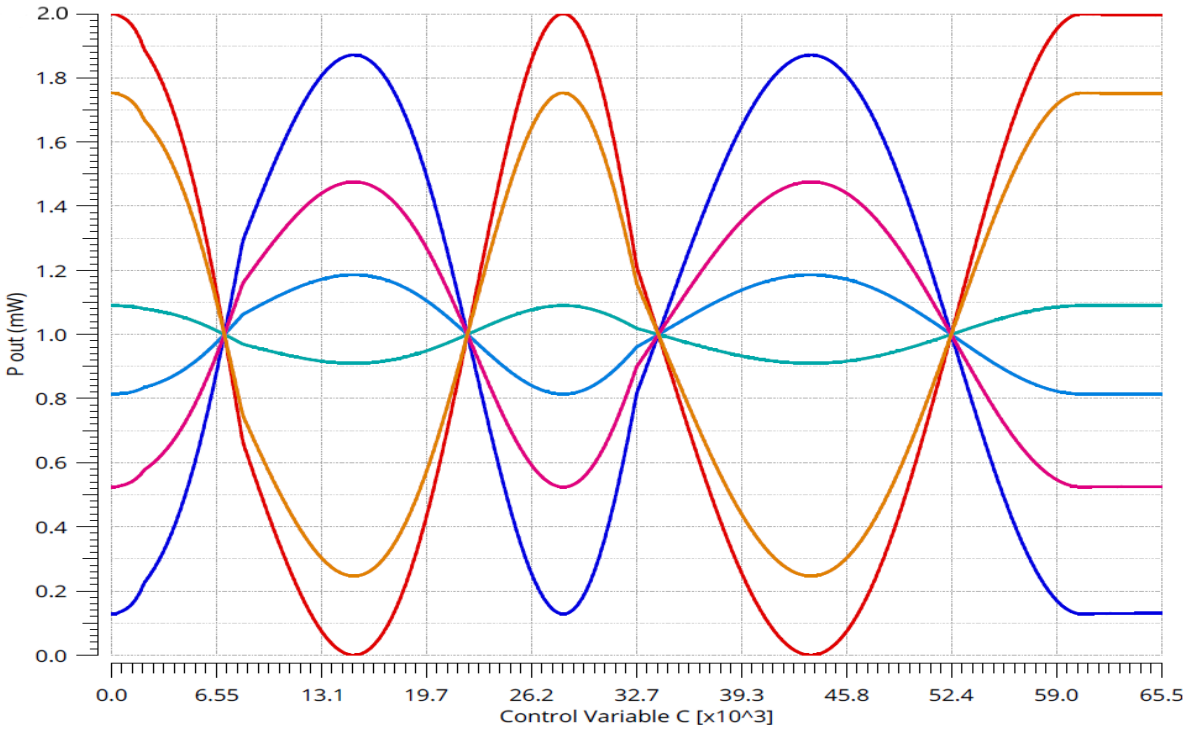
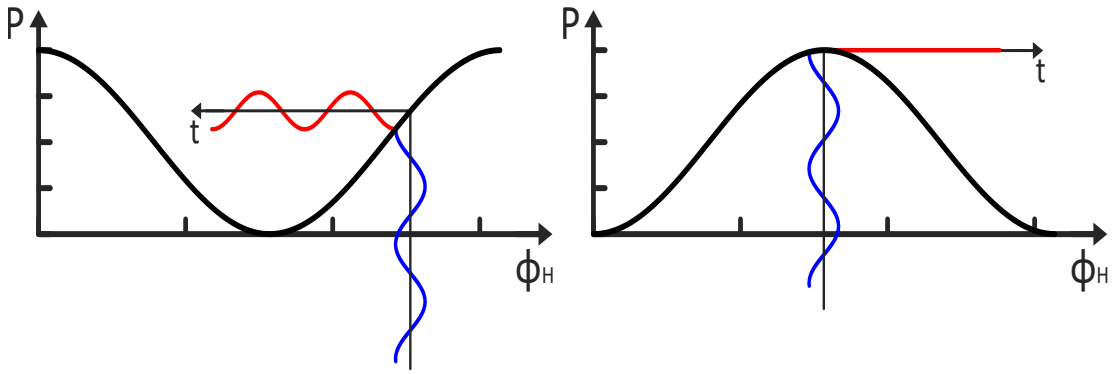


Figure 2.10: Output power of the MZI for 6 different values of V_{H2} (linearly distributed between 0 and 6 V) while the control variable C associated to heater 1 is swept. The "effectiveness" of heater 1 depends on the phase shift induced by V_{H2}, and viceversa.



(a) (b)

Figure 2.11: Schematic representation of dithering: blue is the modulation of phase shift applied by the heater, red signal is the resulting modulation at output. In (**a**) the two signals are in phase, being $\frac{\partial P_{OUT}}{\partial \phi_H}>0$, while in (**b**) the output modulation is nil, since the system is working around a maximum of $P_{OUT}(\phi_H)$.

It is evident, though, that apart from the maxima and minima of the transfer function, other points do exist where both partial derivatives $\frac{\partial P_{OUT}}{\partial \phi_H}$ are nil. These points are the consequence of the interaction between the two control variables (one per heater): there are some working points of an heater that make the other ineffective, as shown in Fig. 2.9b and Fig. 2.10. In a fully analog solution, these points would not represent a problem: they are unstable equilibrium points, and little noise is enough to move the working point to let the feedback loop work properly. The quantization introduced by the ADC in the mixed-signal solution adopted in this work, however, requires some adjustments to deal with this particular situation. How it was managed at digital level will be described in Chapter 4.

2.2.3. Dithering technique

A technique called *dithering*, schematically depicted in Fig. 2.11, is used to extract the information related to the derivative $\frac{\partial P_{OUT}}{\partial \phi_H}$ of the MZI transfer function [17]. The technique, whose name and first utilization date back to the Second World War [18], already proved effective in a number of applications and will be now shortly reviewed.

Single actuator system

To the most simplified degree, *dithering* consists in the application of a small sinusoidal signal v_d, with frequency f_{dith}, upon the control voltage V_H of the heater, thus modulating ϕ_H and, as a consequence, the output power P_{OUT} impinging on the photodiode. If

v_d is sufficiently small, the P_{OUT} modulation will be proportional to the derivative of the MZI transfer function. The information about $\frac{\partial P_{OUT}}{\partial \phi_H}$ can be extracted by means of a demodulation at frequency f_{dith}. It is interesting to observe that such operation preserves the sign of $\frac{\partial P_{OUT}}{\partial \phi_H}$, because while the demodulating signal will always be in phase with respect to v_d, the dithering signal reported on P_{OUT} could be either in phase or in opposition, depending on the sign of $\frac{\partial P_{OUT}}{\partial \phi_H}$.

In an electronic system it is way simpler to generate and demodulate a square wave rather than a sinusoid. It is possible to write the output power as a function of the working point V_{H0} of the heater and the dithering signal v_d.

Considering:

$$V_H(t) = V_{H0} + v_d \cdot sqw(t)|_{f=f_{dith}} \tag{2.5}$$

it is straightforward to write:

$$P_{OUT} \approx P_{OUT}(V_{H0}) + P_d \cdot sqw(t)|_{f=f_{dith}} \tag{2.6}$$

where

$$P_d = v_d \cdot \left.\frac{\partial P_{OUT}}{\partial V_H}\right|_{V_H=V_{H0}}$$

Recalling Eq. 2.4 and Fig. 2.6, it should now be clear why it is convenient to introduce in the system a block implementing something similar to a square root: to have, for two values of ϕ_H separated by 2π (i.e. two working points with the same P_{OUT}), the same amplitude of the dithering modulation, independent from the absolute value of V_H.

Two actuators system

The technique can be easily extended to a system with two heaters by applying two different dithering signals: optical power will be modulated by each square wave according to the respective partial derivative in that particular working point (Fig. 2.9a). The only aspect that requires some care is how to distinguish the two signals when it comes to demodulation: in fact, despite having two heaters, there is only one photodiode, meaning that the two modulations will mix up in the current signal acquired by the analog front-end. The solution is to use two orthogonal[1] signals, either using a different frequency for each modulation or by using two signals in phase quadrature. Both methods have already been proven effective. At the price of higher complexity in the demodulation operation, the former allows to "mark" many different optical beams, each one with its own dithering

[1] In general, two periodic functions f(t) and g(t) with period T are *orthogonal* when $\int_0^T f(t) \cdot g(t)\, dt = 0$.

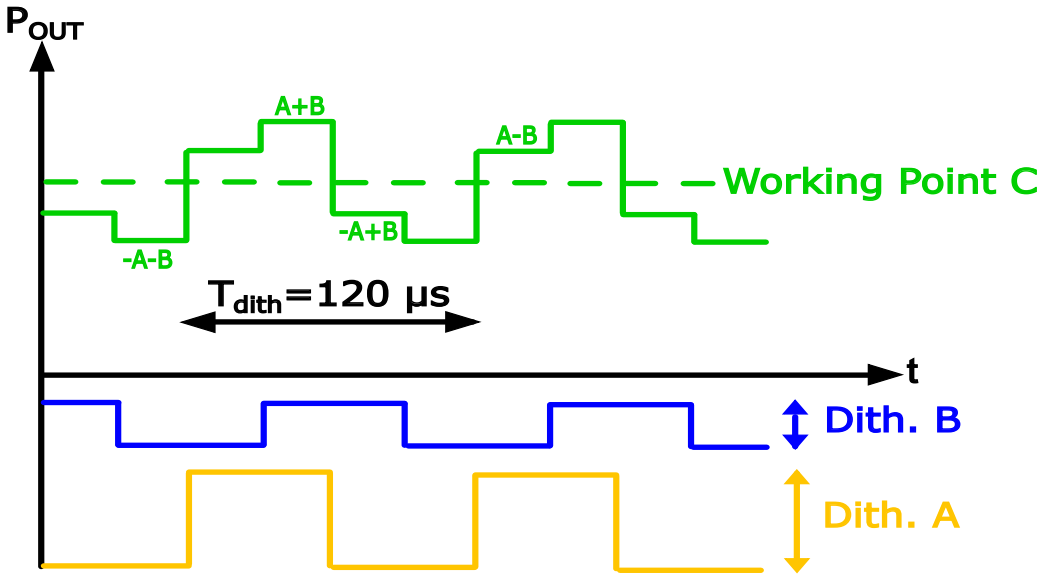


Figure 2.12: Sum of two dithering signals in quadrature, representing the two modulations superimposed to P_{OUT}. It is clear that a demodulating square wave in phase with one of the two will get rid of both offset C and signal in quadrature, while preserving the dithering of interest.

frequency [19], whereas the latter, very simple for what concerns demodulation, can be used only in systems with, at the most, two control variables. Since the Mach-Zehnder Interferometer has two actuators, and every device of the mesh is stabilized independently from the others, the solution adopted in this work is the modulation with two square waves in quadrature (Fig. 2.12). It is also interesting to observe that, when a MZI is locked to a point where $\frac{\partial P_{OUT}}{\partial \phi_H} = 0$ is true for both partial derivatives, no residual modulation is passed to the next interferometer, meaning that *mesh* can be stabilized sequentially, one interferometer after the other.

2.3. Evaluation of the loop gain

At this point it might be useful to try to evaluate the loop gain for a particular yet very relevant working point of the optical component, that is when the system is locked to a minimum of the optical power impinging on the photodiode. For example, this is the working point of every MZI in the mesh when the system is used as a Self-Aligning Beam Coupler, presented in Chapter 1: the goal is to bring the 100 Hz bandwidth demonstrated in the previous design, which was a fully analog-chip relying on transparent detectors [12], up to the kHz range. As it will be shown, this is possible only thanks to the adoption of

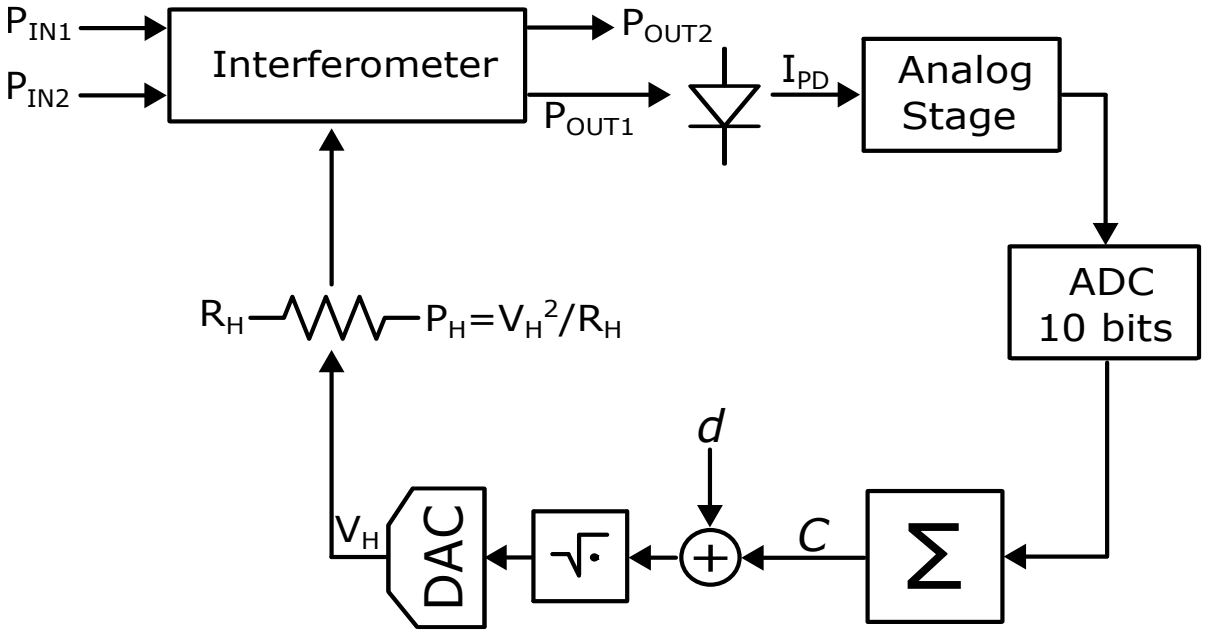


Figure 2.13: Scheme for loop gain evaluation

photodiodes combined with some digital signal processing.

Particular care has to be put in the description of two blocks of the loop gain:

- The integrator, which operates in the discrete-time domain and at digital level, should be reported, with proper approximations, to its Laplace transform.
- The optical response of the system to the variations of the power P_H dissipated by the heater, already described in Sec. 2.1, has to be evaluated even more carefully in this situation where, in principle, $P_d = v_d \cdot \frac{\partial P_{OUT}}{\partial V_H} = 0$

A schematic representation of the control loop, involving all the relevant blocks for the loop gain evaluation, is shown in Fig. 2.13. The contribution of each block will now be analyzed in detail to determine G_{LOOP}, which is determined by cutting the loop after the integrator and applying a small variation ΔC on the current working point C.

An important remark has to be made before starting: the system is supposed to work with an **ideal** square-root operation being performed between the control variable C and the 12 bits digital word fed to the DAC: the consequence is that the quadratic non-linearity highlighted in Eq. 2.2 disappears, and the response of the optical system becomes independent from the absolute position V_H of the minimum. It is also important to observe that, as a consequence of the algorithm that digitally implements the algorithm, for a given value of C+d what is extracted is $3 \cdot \sqrt{C+d}$, thus introducing a factor 3 in the loop gain.

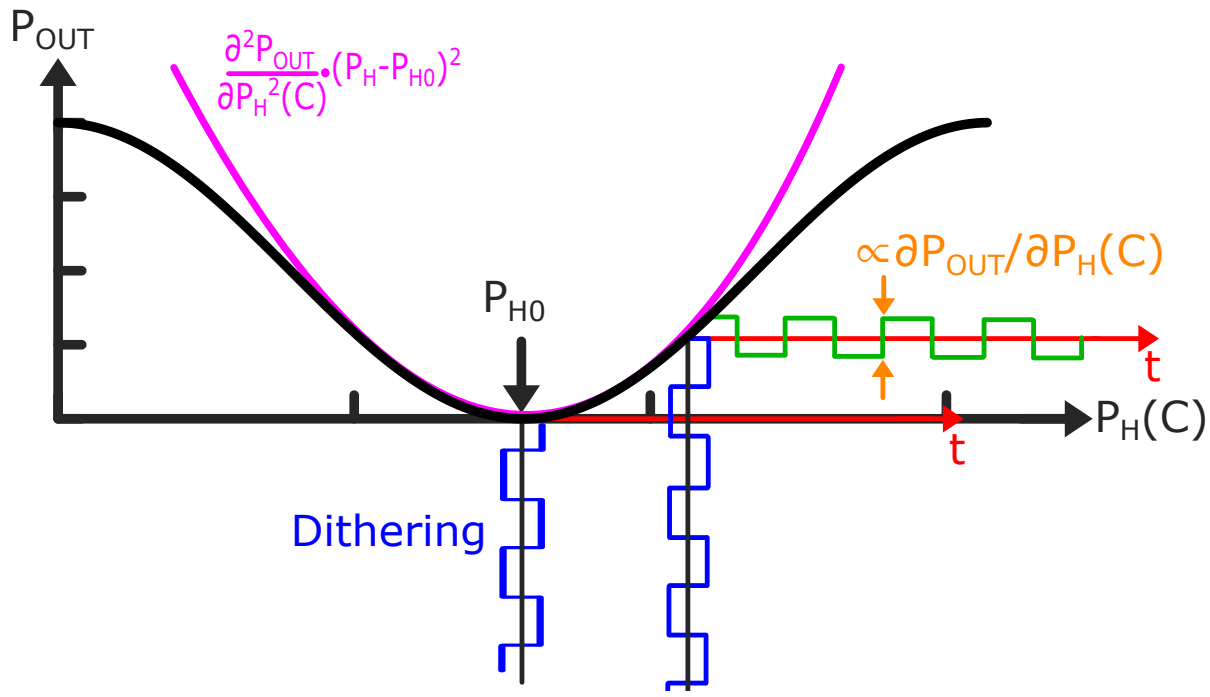


Figure 2.14: Variation of P_d as the working point of the device is moved from a minimum of the transfer function

Optical system response

Focus should be first placed on how the optical system reacts to a variation of the state variable C, and as a consequence of the power $P_H = \frac{V_H^2}{R}$ dissipated by the heater. It is important to observe that the error signal that is integrated in the loop is the dithering amplitude P_d reported at the output of the MZI, meaning that the "gain" of the optical system to be considered is $\frac{\partial P_d}{\partial C}$. From Fig. 2.14 and Eq. 2.6, it is evident that, if P_{H0} is the heater power corresponding to a minimum of the MZI's transfer function, then $P_{OUT}(P_H)$ can be approximated, for small variations, with its second derivative, since around P_{H0} also $\frac{\partial P_{OUT}}{\partial P_H}$=0 holds:

$$P_{OUT}(P_H) = \frac{\partial^2 P_{OUT}}{\partial P_H^2} \cdot (P_H - P_{H0})^2 \tag{2.7}$$

Where it should be recalled that, since a square root operation is done, P_H can be written as:

$$P_H = \frac{V_H^2}{R_H} = \frac{(3 \cdot \sqrt{C+d} \cdot \frac{6\,V}{2^{12}})^2}{R_H} \tag{2.8}$$

$\frac{6\,V}{2^{12}}$ being the conversion factor between the digital word fed to the DAC and its analog output V_H and d the amplitude of the digital dithering modulation superimposed to C.

Some boring math now has to be done. In fact, the output power can be written as:

$$\begin{aligned} P_{OUT}(P_H) &= \frac{\partial^2 P_{OUT}}{\partial P_H^2} \cdot (P_H - P_{H0})^2 \\ &= \frac{R_H^2}{S_D} \cdot \frac{\partial^2 I_{PD}}{\partial (V_H^2)^2} \cdot \left[\frac{9(C+d)(\frac{6\,V}{2^{12}})^2}{R_H} - P_{H0} \right]^2 \\ &= \frac{R_H^2}{S_D} \cdot \frac{\partial^2 I_{PD}}{\partial (V_H^2)^2} \cdot \left[\left(\frac{9d \cdot (\frac{6\,V}{2^{12}})^2}{R_H} \right)^2 + \left(\frac{9C \cdot (\frac{6\,V}{2^{12}})^2}{R_H} - P_{H0} \right)^2 \right. \\ &\left. + 2 \cdot \left(\frac{9d \cdot (\frac{6\,V}{2^{12}})^2}{R_H} \right) \cdot \left(\frac{9C \cdot (\frac{6\,V}{2^{12}})^2}{R_H} - P_{H0} \right) \right] \end{aligned} \tag{2.9}$$

where S_D is the *radiant sensitivity* of the photodiode ($S_D = \frac{I_{PD}}{P_{OUT}}$) and highlighted in red is the quadratic contribution due to the small dithering variation, which can be considered negligible.

At this point, it is possible to conclude that P_d, i.e. the amount of optical power determined by the dithering signal, can be isolated from Eq. 2.9 as:

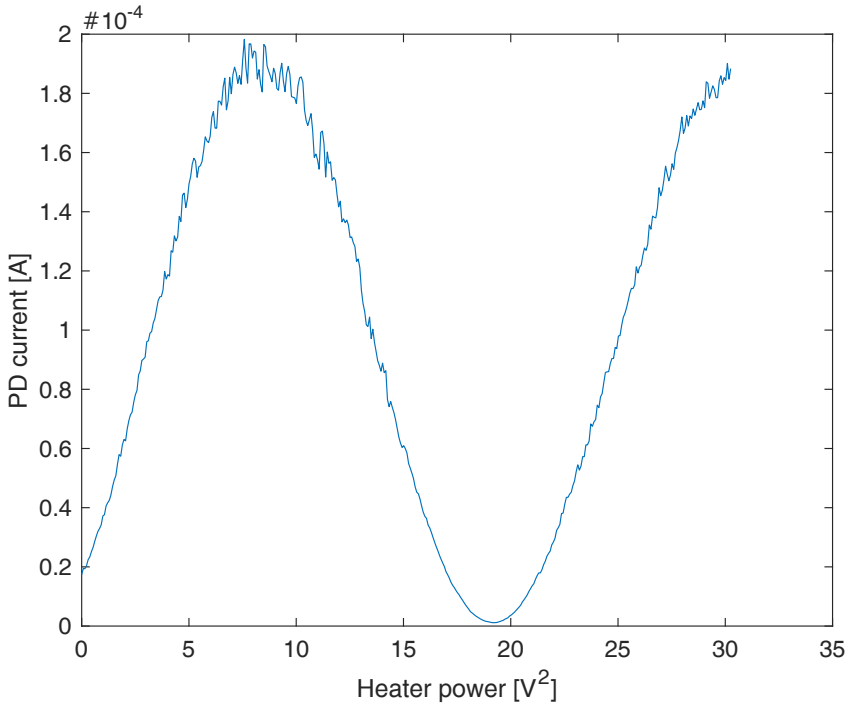
$$P_d = \frac{\partial^2 I_{PD}}{\partial (V_H^2)^2} \cdot \frac{R_H^2}{S_D} \cdot 2 \cdot \left(\frac{9d \cdot (\frac{6\,V}{2^{12}})^2}{R_H} \right) \cdot \left(\frac{9C \cdot (\frac{6\,V}{2^{12}})^2}{R_H} - P_{H0} \right) \tag{2.10}$$

There is only one final move to be done in order to derive the gain of the optical element: to compute $\frac{\partial P_d}{\partial C}$, i.e. the variation of the photodiode-referred dithering amplitude P_d when the system is moved by a space ∂C from the minimum of the transfer function (where obviously $\frac{\partial P_d}{\partial C}$=0). The result is:

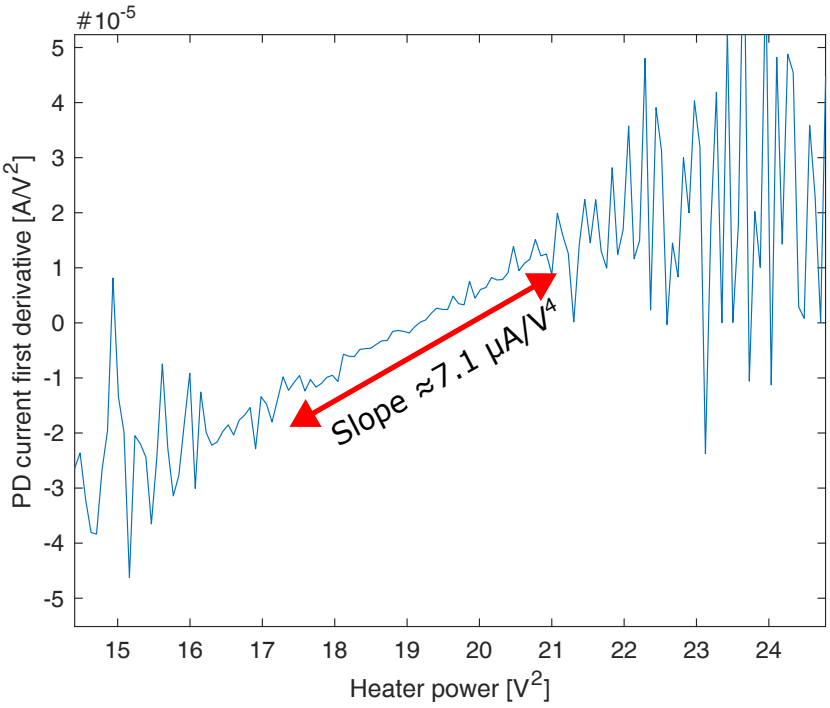
$$\begin{aligned} \frac{\partial P_d}{\partial C} &= \frac{\partial^2 I_{PD}}{\partial (V_H^2)^2} \cdot \frac{R_H^2}{S_D} \cdot 2 \cdot \left(\frac{9d \cdot (\frac{6\,V}{2^{12}})^2}{R_H} \right) \cdot \left(\frac{9 \cdot (\frac{6\,V}{2^{12}})^2}{R_H} \right) \\ &= \frac{\partial^2 I_{PD}}{\partial (V_H^2)^2} \cdot \frac{162}{S_D} \cdot \left(\frac{6\,V}{2^{12}} \right)^4 \cdot d \end{aligned} \tag{2.11}$$

Unsurprisingly, Eq. 2.11 shows that:

- $\frac{\partial P_d}{\partial C}$ increases with the dithering amplitude d. It is not strange: applying a larger perturbation around a point where $\frac{\partial P_{OUT}}{\partial P_H}$=0 leads to the approximation of the first derivative with a larger value, as long as the perturbation is sufficiently small.
- $\frac{\partial P_d}{\partial C}$ is **proportional** to d and **independent** from the working point C: this is exactly the effect of the square root described in Sec. 2.1.2.



(a)



(b)

Figure 2.15: (**a**) Measured output current of the photodiode and (**b**) its first derivative, from which it is possible to evaluate the second derivative around the value of V_{H0} corresponding to a minimum of the transfer function.

With d being set externally according to the requirements of the application and S_D declared in the photodetector datasheet ($\approx 0.85\frac{A}{W}$), the only variable left to be determined is the second derivative of the $I_{PD}(V_H^2)$ MZI transfer function, which obviously depends on the total amount of power circulating in the waveguides. $\frac{\partial^2 I_{PD}}{\partial V_H^4}$ can be extracted by the measurement done in Fig. 2.3, where 1 mW (0 dBm) of optical power is injected from the fiber into the MZI, with -7 dB of insertion losses. In this case, the estimation leads to $\frac{\partial^2 I_{PD}}{\partial V_H^4} = 7.1\,\frac{\mu A}{V^4}$ (Fig. 2.15).

Photodiode, Analog Stage and ADC

The optical signal impinges on a photodiode that turns it into a current by means of the already presented proportionality constant called *radiant sensitivity* (S_D):

$$I_{PD} = S_D \cdot P_{OUT} \tag{2.12}$$

After that, the current signal enters the analog stage and undergoes an amplification via a transimpedance amplifier and ends up charging the capacitor of a gated integrator, that produces the output value to be sampled by the ADC. The gain of this block can thus be written as:

$$G_{TIA} = \frac{R_F}{R} \cdot \frac{T_G}{C_G} \tag{2.13}$$

With T_G (duration of the integration) being fixed to $\approx$9.55 μs. As it will be shown in further detail in Ch. 3, G_{TIA} may have different values according to the amount of output current delivered by the photodiode. In the case the MZI is working close to a minimum, as it is considered in this analysis, the gain of the stage is $G_{TIA} \approx 3.6\,M\Omega$.

The ADC turns the analog value produced by the gated integrator into a 10 bits word. Adopting the power supplies ($\pm 1.65\,V$) as reference voltages, the transformation factor from the analog to the digital domain is:

$$G_{ADC} = \frac{2^{10}}{3.3\,V} \tag{2.14}$$

Integrator

The ADC is supposed to work at a sampling frequency f_s=100 kHz. It means that the signal $x_s(t)$ fed to the integrator (Fig. 2.16) can be seen as a comb of Dirac pulses, with

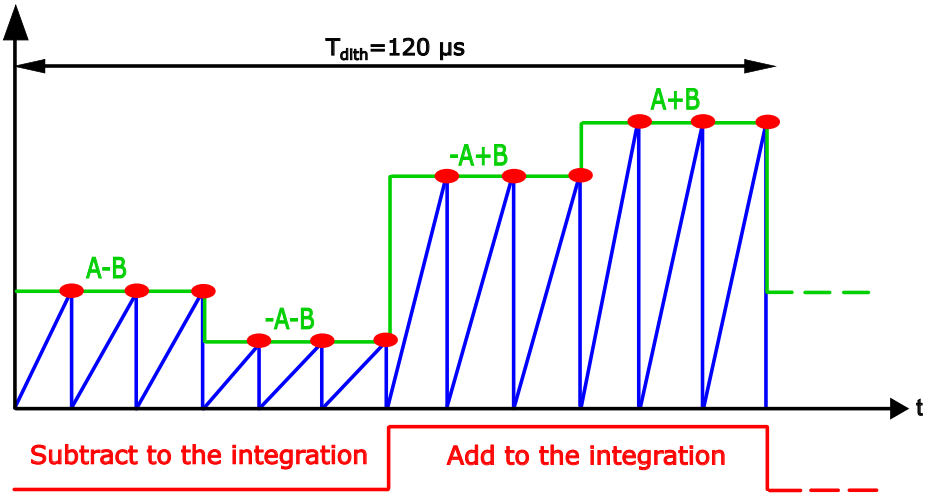


Figure 2.16: Schematic representation of dithering waveforms: photodiode current signal (green), voltage signal *x(t)* at the ADC input (blue) and sampled signal x_s at the output of the ADC (red). The demodulation considered here (red) allows the extraction of dithering amplitude B while rejecting A as well as the average value.

each dithering period being represented by 12 δ-pulses:

$$x_s(t) = \sum_n x(nT) \cdot \delta(t - nT) \tag{2.15}$$

It can also be shown, by applying the definition, that the Laplace transform $X_s(s)$ of the sampled signal is:

$$X_s(s) = \frac{1}{T} \sum_{n=-\infty}^{n=+\infty} X(s - jn\frac{2\pi}{T}) \tag{2.16}$$

where $X(s)$ is the Laplace transform of the continuous-time signal $x(t)$.

Eq. 2.16 shows a very well known result: the $\mathcal{L}$-transform of a sampled signal is the periodic replica, with periodicity f_s, of the $\mathcal{L}$-transform of the continuous time signal. Aliasing is not critical, since the fundamental harmonic of the signal is located at $f_{dith} = \frac{f_S}{12}$; in addition to that, $X(s)$ is the result of the low-pass filtering action of the gated integrator, that completes the analog stage before the ADC, and introduces with respect to noise an equivalent pole at $\frac{1}{\pi T_G} \approx 33\,\text{kHz}$ [20], as shown in Fig. 2.17.

$x_s(t)$ is fed to the integrator, whose transfer function in the discrete-domain is:

$$H(z) = \frac{1}{z - 1} \tag{2.17}$$

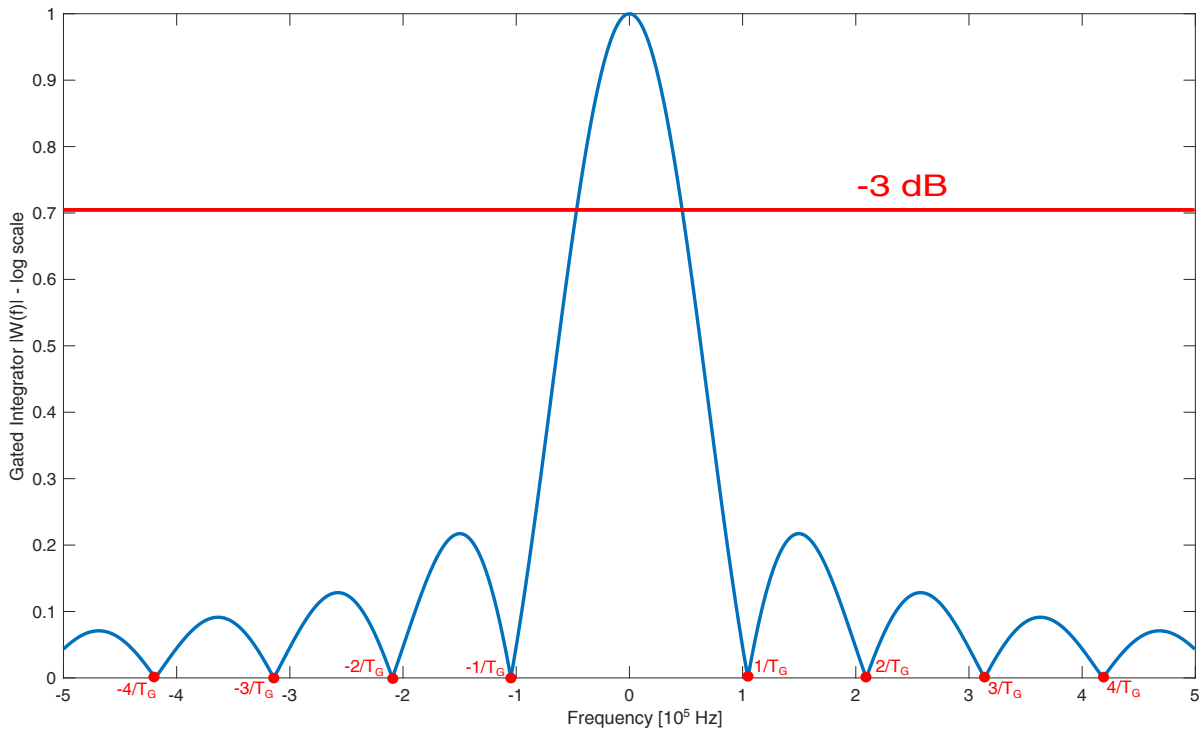


Figure 2.17: Frequency-domain representation of the weighting function of a gated integrator

However, the $\mathcal{L}$-transform can be seen as a particular case of the $\mathcal{Z}$-transform. The equivalence that allows to write the $\mathcal{L}$-transform of the discrete-time integrator is:

$$H(s) = H(z)|_{z=e^{sT}} = \frac{1}{e^{sT}-1} \approx \frac{1}{sT} \tag{2.18}$$

where the last approximation holds in case sT«1, which is verified since the dithering modulation has a periodicity of T_{dith}=120 μs, whereas the samples are taken every T=10 μs - 12 times faster.

After the integrator, the loop is complete and the loop gain for the particular condition of the MZI locked on a minimum of its transfer function can be assessed as:

$$\begin{aligned} G_{LOOP} &= \frac{\partial P_d}{\partial C} \cdot S_D \cdot G_{TIA} \cdot G_{ADC} \cdot \frac{K_{BW}}{sT} \\ &= \frac{\partial^2 I_{PD}}{\partial V_H^4} \cdot 162 \cdot (\frac{6\,V}{2^{12}})^4 \cdot d \cdot 3.6\,M\Omega \cdot \frac{2^{10}}{3.3\,V} \cdot \frac{K_{BW}}{sT} \end{aligned} \tag{2.19}$$

G_{LOOP} depends on one parameter that may change from an application to another, i.e. $\frac{\partial^2 I_{PD}}{\partial V_H^4}$, and two parameters that can be set at digital level:

- the dithering amplitude d;
- a *integration gain* K_{BW}, which makes possible to adjust the closed-loop bandwidth of the system by changing the weight of the samples fed to the integrator.

With $d = 2^{10}$ (C, as indicated in Fig. 2.13, is 21 bits wide) and $K_{BW} = 1$, the closed-loop bandwidth of the system is estimated at $f_{0dB} \approx$600 Hz. Thanks to the possibility of a tunable bandwidth (acting either on d or K_{BW}) the system can address different operating conditions, that may range from rejecting slow thermal drifts (in the order of few Hz) to tracking external stimuli injected on purpose in the interferometer, up to 1-2 kHz, an upper limit being set by the dithering frequency at $f_{dith} = \frac{f_s}{12} \approx$8.3 kHz. It is also possible to compensate any bandwidth variation due to different values of $\frac{\partial^2 I_{PD}}{\partial V_H^4}$, a parameter which is ultimately set by the total amount of optical power circulating in the photonic chip.

3 | Analog Front-End

Introduction

The very first stage after each Mach-Zehnder interferometer is an analog front-end, schematically portrayed in Fig. 3.1. It is meant to extract the dithering signal from the light impinging on the photodiode at the end of the "blind" branch of the interferometer.
The generated current signal is first amplified and then integrated in order to deliver at the ADC input a new sample every 10µs. The feedback network of the stage has a variable gain, so as to always be able to amplify and filter the signal with the proper required resolution and no risk of saturation. A gated integrator is the analog filter adopted to keep white noise well below the quantization noise of the ADC.
Different requirements were considered in the two parts of the design: while keeping noise low was crucial in the first amplifier, minimal power dissipation was targeted in the second one.

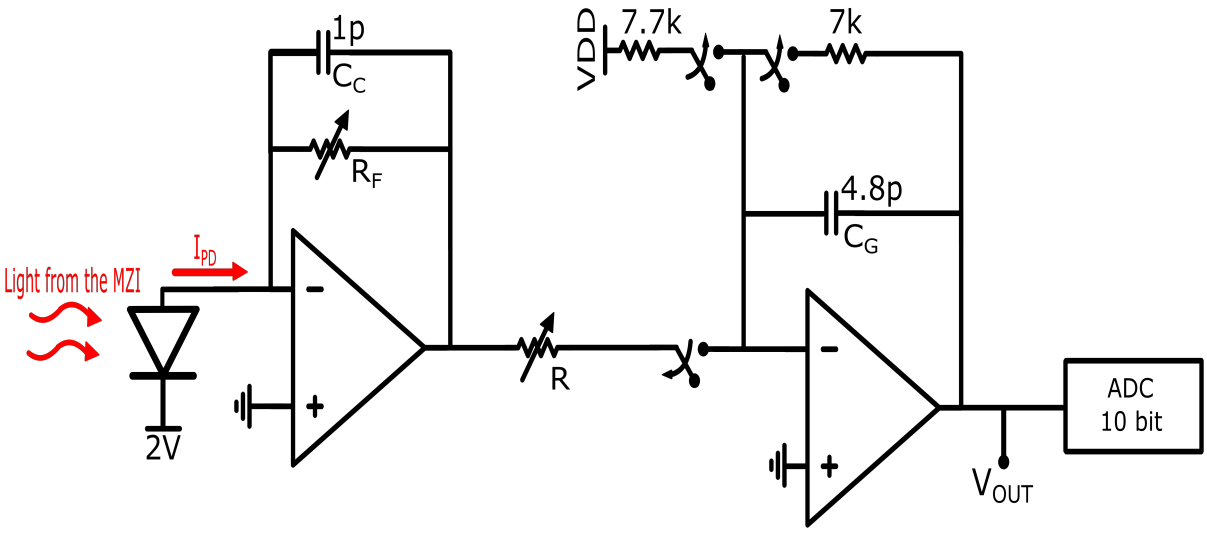


Figure 3.1: Schematic representation of the input stage

3.1. Transimpedance amplifier

3.1.1. Photodiode

The photodiode adopted in this work is the *Ge_PowMonitor_Cband*, a Ge-based photodetector available in the AMF technology. Three fundamental parameters are needed for the characterization of the device: bandwidth, responsivity and dark current. They are all reported in the datasheet for a 2 V reverse polarization, which is also the voltage drop applied to the diode in this application, and around a wavelength $\lambda = 1550$ nm, a standard one for photonics.

- **Responsivity** (S_D): also known as *radiant sensitivity* and already presented in Chapter 2, it is the ratio between impinging optical power and output current. The declared value is 0.85 A/W. In the hypothesis of having up to 1 mW (0 dBm) of power on the photodiode, the analog stage should be able to handle currents as large as 850 µA.
- **Dark current**: it is the current due to the carriers' thermal generation events, which are not related to photon absorption, thus constituting an unwanted baseline for the signal. Such current (≈150 nA) corresponds to roughly 180 nW (-37 dBm) of equivalent optical power on the photodiode. This is one of the main motivations behind the adoption of a dithering-based control mechanism: in order to minimize the light reaching the detector below -40 dBm, the state variable to be monitored cannot be the absolute working point of the MZI, but its derivative, which is obviously independent from whatever offset.
- **Bandwidth**: it is the maximum frequency at which the device output current can follow light intensity variations, and it is estimated to be >12 GHz, at least two orders of magnitude beyond whatever other singularity in the loop gain.

The photodiode can be modelled as:

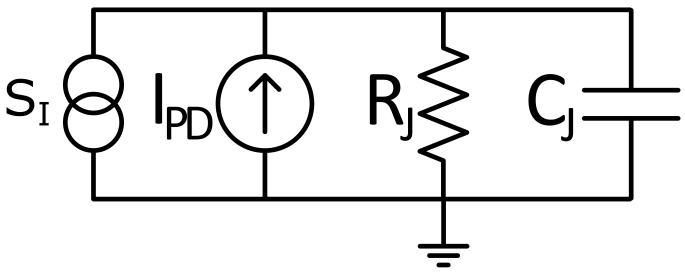


Figure 3.2: Electrical model of a photodiode

where R_J is the shunt resistance of the device (i.e. the slope of its I-V curve around bias point) and C_J the junction capacitance, determined by the dimensions of the detector (which are comparable to those of the waveguides, $\approx 0.1\,\mu m^2$). Since R_J is typically >10MΩ and C_J is not bigger than few fF (well below the $1\,pF$ parasitic capacitance assumed for the connection to the ASIC), both parameters are negligible when it comes to noise computations.

As a final remark, it is worth recalling that the shot noise related to the photodiode current can be considered as white and its power spectral density can be expressed as:

$$S_I = 2qI_{PD} \tag{3.1}$$

3.1.2. Variable gain through switching resistive network

Variable gain

The input stage has to handle input currents between 850 µA, when a maximum power of 1 mW (0 dBm) is impinging on the photodiode, and 150 nA, in the ideal case where only the dark current flows in the device. In terms of input-referred resolution of the 10 bit ADC, this would correspond to a current LSB of $LSB_{I_{PD}} = \frac{850\,A}{2^{10}} \approx 830$ nA. This value also represents the minimum current variation in the photodiode needed by the ADC in order to discriminate between two different samples: in practice, the amplitude of the dithering signal should be large enough to cause the current to change at least by 830 nA. However, this would be equivalent to having a ≈ -31 dBm variation of optical power in the waveguide, way larger than the -40 dB *extinction ratio*[1] targeted in this project.

The problem of the limited ADC resolution was solved by splitting the current range into 6 different regions. Considering a DC current I_{PD} flowing in the photodiode, the transimpedance of the stage can be written as:

$$G_{IN} = \frac{R_F}{R} \cdot \frac{T_G}{C_G} \tag{3.2}$$

with T_G being the integration time of the gated integrator, set to $\approx 9.55\,\mu s$, i.e. 10.5 out of the 11 clock cycles of each sampling period. The remaining 0.5 cycles are used for the reset of the integration capacitance C_G=4.8 pF. With a clock frequency of f_{CLK}=1.1 MHz, the resulting sampling period is 10 µs. The integration time, that determines 12 sampling events per dithering period, is dictated by the necessity of limiting the size of C_G: a longer

[1] The ratio between the peak of the transfer function, conventionally set to 0 dBm, and its minimum.

integration time would require a larger capacitor or a larger R.

Tab. 3.1 reports the different values of the components and the resulting G_{IN}.

Region	$I_{PD_{MAX}}$[µA]	$I_{PD_{min}}$[µA]	R_F[kΩ]	R[kΩ]	G_{IN}[Ω]
1	850	212.5	1.4	800	3.5 k
2	212.5	53.12	5.6	800	14 k
3	53.12	13.28	22.4	800	56 k
4	13.28	3.32	44.8	400	224 k
5	3.32	0.83	179.2	400	896 k
6	0.83	0.15 (Dark current)	358.4	200	3.58 M

Table 3.1: Different gains depending on the light intensity impinging on the photodiode

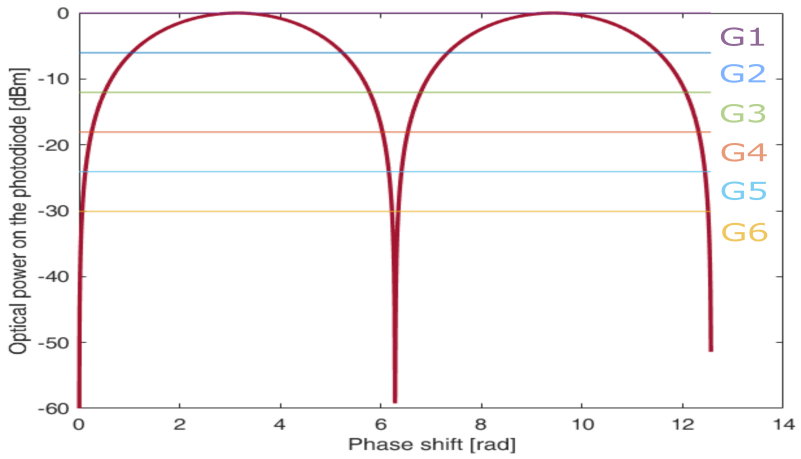


Figure 3.3: Power on the photodiode (log scale) as a function of the relative phase shift induced in the waveguides of the MZI

It is possible to observe that both current (max and min) and gain values are progressively scaled by a factor 4 from one to another: it means that all regions of current/optical power cover the same interval of V_{OUT}=[VSS + 0.15 V; VDD - 0.15 V], the 150 mV margin being set by the output voltage swing of the second amplifier. This variable gain is *de facto* implementing a "zoom" on the transfer function of the interferometer, graphically represented in Fig. 3.3: as the heaters drive the device towards the minimum, the 10 bits of the ADC are used to map a narrower range of current values, allowing for an improvement on the resolution. As a result, the very last region has an equivalent current LSB of $LSB_{I_{PD}} = \frac{830\,nA}{2^{10}} \approx 810$ pA, corresponding to ≈-61 dBm of optical power: it allows

to apply a dithering signal that, despite being way larger than the LSB, will keep the MZI within an acceptable working region.

Finally, the choice of a power of 2 as a scaling factor between the operating regions will come into help when dealing with the ADC samples in the digital part of the system.

Resistive switching network

Any variation in the gain of the stage is determined by adjusting the $\frac{R_F}{R}$ ratio. The regulation happens automatically at digital level, by setting two different thresholds (upper and lower, and the same for every G_{IN}) on the samples produced by the ADC, as it will be shown in Chapter 4. Looking at the values reported in Tab. 3.1, one might think that the resistive network should be made just with two resistors, $R_F = 800\,k\Omega$ and R=358.4 kΩ, and the switches needed to split the resistors and implement the different values of the gain.

It is possible to adopt a smarter solution, shown in Fig. 3.4: moving from the lowest to the highest gain, R_F increases from 1.4k Ω to 358.4 kΩ, whereas R decreases from 800 kΩ down to 200 kΩ. As a consequence, some resistance could be shared between the two by implementing resistors with proper dimensions and a boolean digital network to drive the switches. The parallel network with five 5.6 kΩ resistors is needed to overcome accuracy issues that would arise for placing just one single 1.4 kΩ component.

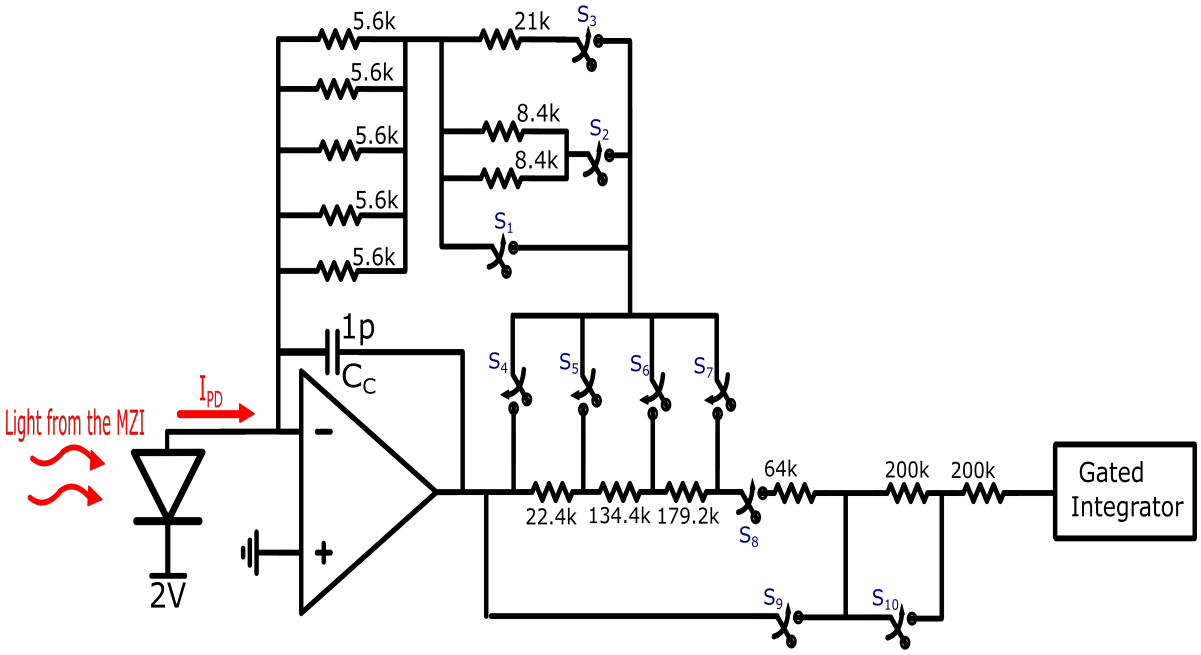


Figure 3.4: Switching resistive network implementing the variable gain of the stage

Selected G_{IN}	A	B	C	Switches closed
1	0	0	0	S_1, S_4, S_8
2	0	0	1	S_2, S_4, S_8
3	0	1	0	S_3, S_4, S_8
4	0	1	1	S_3, S_5, S_9
5	1	0	0	S_3, S_6, S_9
6	1	0	1	S_3, S_7, S_9, S_{10}

Table 3.2: Combinational logic driving the variable gain of the input stage

Having 6 different values of G_{IN}, a 3 bit combinational logic is needed to properly turn on and off the switches. Its truth table can be optimized to derive the logical network with minimal area occupation: looking at Tab. 3.2, one can conclude that, for example, S_{10} is driven exactly like S_7, or that S_4 is paired with S_8 and opposite to S_9.

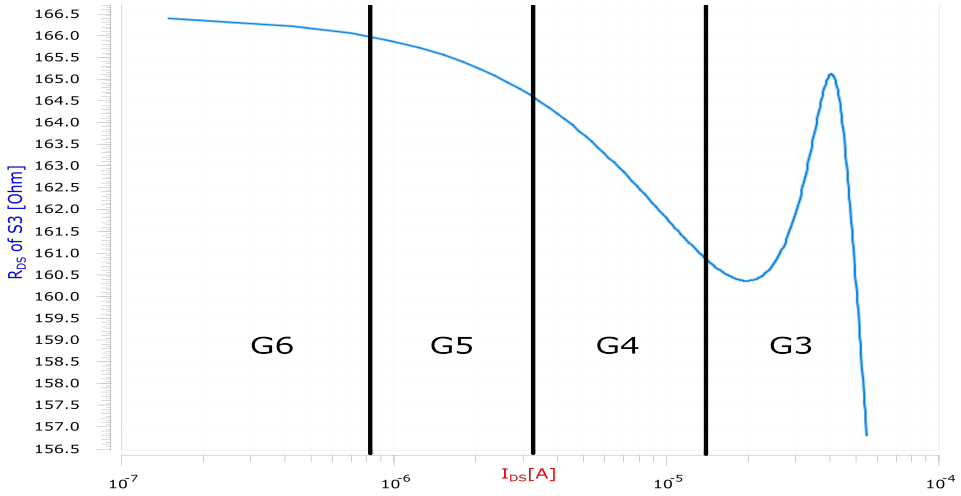


Figure 3.5: On resistance of switch S_3

A couple of final remarks should be made at this point:

- The adoption of this resistive network saved at least 300 kΩ. Since these components are integrated using highly-resistive polysilicon (*rpolyh* is the model's name in the technology AMS C35B4 used in the project), and considering the minimum high precision width of 2 µm, with a typical sheet resistance of 1.2 kΩ/square it is possible to say that at least 1'000 μm^2 of area occupation per channel have been saved.
- In the schematic reported in Fig. 3.4 the switches are assumed ideal, i.e. with zero on-resistance. In the actual design they are implemented as transmission gates, whose resistance is in the order of a few hundreds of Ω: as a result, the actual

resistors are slightly smaller than those in Fig. 3.4. As an example, Fig. 3.5 reports the simulated $R_{DS_{ON}}$ of S_3, which is closed for the 4 largest values of G_{IN}. In particular, for G_6 the variations are well within 1% of the absolute value.

3.1.3. OTA

The design chosen to implement the first amplifier of the chain is a 2-stage, current compensated transconductance amplifier, reported in Fig. 3.6. All the parameters of the transistors are reported in Tab. 3.3.

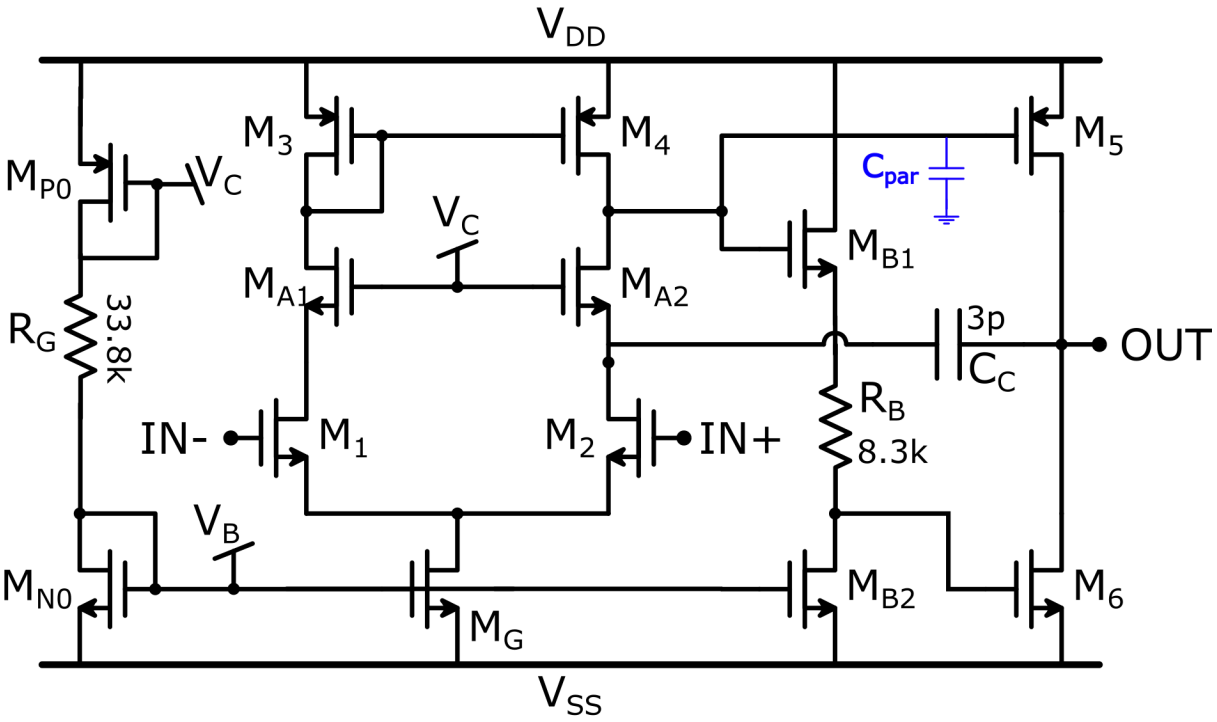


Figure 3.6: Schematic of the OTA and the polarization network for the amplifier of the first stage

First of all, a simple yet very stable topology has been chosen to generate the bias for the tail generator (V_B) and the current buffer transistors in cascode configuration (V_C). For example, if the MOSFETs were larger than the expected value, they could carry more current; however, this would cause a larger voltage drop onto R_G, leading to a reduction of V_{GS_N} and V_{SG_P} as well as of the current in the branch, implicitly implementing a negative feedback. With the sizing adopted in the design, gate voltages are fixed to V_C=0.73 V and V_B=-0.97 V.

$M_{B1,2}$ are biased with the help of a resistor R_B, as the voltage drop required between the source of M_{B1} and the drain of M_{B2} is below the typical threshold voltage of the

Device	$\lvert V_T \rvert$ [V]	$\lvert V_{OV} \rvert$ [V]	$\lvert V_{DS} \rvert$ [V]	I_{DS} [μA]	W [μm]	L [μm]	g_m [μS]	r_0 [kΩ]
M_{n0}	0.53	0.15	0.68	50	34	1.2	560	600
M_{p0}	0.72	0.20	0.92	50	60	1.2	450	450
M_g	0.53	.15	0.75	200	128	1.1	2250	155
$M_{1,2}$	0.72	0.17	0.63	100	100	1.2	1000	300
$M_{3,4}$	0.72	0.4	1.13	100	30	1.2	500	240
$M_{A1,A2}$	0.88	0.12	0.80	100	56	0.7	1300	180
M_{B1}	0.88	0.15	2.1	50	34	1.2	570	1400
M_{B2}	0.53	0.15	0.78	50	34	1.2	570	1400
M_5	0.72	0.40	1.65	800	225	1.1	3640	44
M_6	0.53	0.25	1.65	800	180	1	5770	58

Table 3.3: Fundamental parameters of all the MOS devices in the schematic of the OTA

devices, making it impossible to substitute the resistor with a MOSFET in transdiode configuration.

The different threshold voltages between the n-type MOSFETs are the result of *body effect*, being the body of these transistors always shorted to VSS (the potential of the substrate, which is slightly p-doped), whereas the source might be at different potentials; this effect is not present for p-type devices, whose body is always connected to source.

Finally, the relatively high power consumption (≈3.6 mW) is mainly due to the large current in the second stage, necessary to connect the amplifier to the photodiode, whose impinging optical power may generate currents as large as 850 μA.

Open-loop gain and closed-loop stability

Bode plots of the open-loop gain of the amplifier for different values of G_{IN} are reported in Fig. 3.7.

The DC gain G(0) is obtained multiplying the gain of the differential stage and that of the output stage, resulting in:

$$G(0) = G_1(0) \cdot G_2(0) = (g_{m1} r_{04}) \cdot [(g_{m5} + g_{m6})(r_{05} \parallel r_{06})] \tag{3.3}$$

It is worth mentioning that the gain of the differential stage is boosted by the fact that the resistance seen towards the drain of the current buffer transistor M_{A2} is improved by a factor $g_{mA2} r_{0a2}$. The low frequency pole of the stage is the one introduced by the Miller

capacitance:

$$f_{LFP} \approx \frac{1}{2\pi C_c\, r_{04}(g_{m5}+g_{m6})(r_{05} \parallel r_{06})} \tag{3.4}$$

As a result, the GBWP will be set at

$$GBWP = G(0) \cdot f_{LFP} = \frac{g_{m1}}{2\pi C_C} \tag{3.5}$$

The buffer's finite transconductance also introduces a LHP zero at

$$f_Z = \frac{2 \cdot g_{mA}}{2\pi C_c} \tag{3.6}$$

Finally, the Ahuja compensation also introduces two complex conjugate poles, whose natural frequency and Q-factor are ([21], [22]):

$$f_0 = \frac{1}{2\pi} \cdot \sqrt{\frac{(g_{m5}+g_{m6})g_{mA}}{C_L C_{par}}} \text{ and } Q = \frac{C_C}{C_C + C_L}\sqrt{\frac{g_{m5}+g_{m6}}{g_{mA}} \cdot \frac{C_{par}}{C_L}} \tag{3.7}$$

where C_{par} is the parasitic resistance seen towards ground at the high impedance output of the differential stage (gate of M_5). The value resulting from simulation is C_{par} ≈1 pF, mainly due to the large area occupied by M_5 and M_6. The value of the load capacitance considered here is C_L=1 pF of the compensation capacitance. This sizing sets G(0)≈ 92.3 dB, $f_{LFP} \approx 1.2\,kHz$, GBWP≈50 MHz, $f_Z \approx 140$ MHz, $f_0 \approx 300$ MHz and Q≈2.

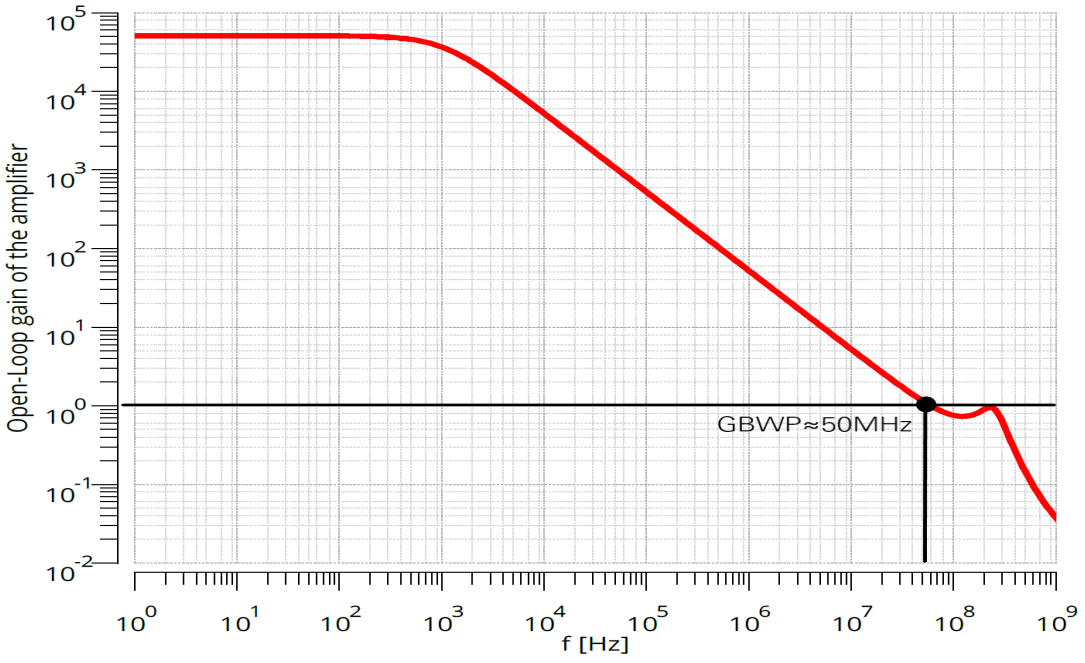


Figure 3.7: Open loop gain of the first OpAmp of the chain

Despite the resonant peak being very close to GBWP, as highlighted in Fig. 3.7, the amplifier will never be used in buffer configuration, as it will be shown in the following, thus preserving the stability of the stage.

Regarding closed-loop stability, a remark should be made on the addition of the 1 pF capacitance C_C in parallel to the feedback resistor. This capacitance is needed to introduce a zero in the loop-gain of the amplifier: without such component, the input parasitic capacitance C_{IN} (due to the connection of the photodiode to the chip) would add a pole to the loop gain that, not being compensated, might lead to poor phase margin and instability. Such parasitism is the sum of the input capacitance of the amplifier (<100 fF) and the parasitic one coming from the connection of the photodiode to the chip, assumed at ≈1 pF. Thanks to the addition of C_C, the open-loop transfer function from V_{OUT} to the "-" node of the amplifier in the circuit of Fig. 3.8 becomes

$$\frac{V\text{-}}{V_{OUT}} = \frac{1 + sC_C R_F}{1 + s(C_C + C_{IN})R_F} \tag{3.8}$$

If $C_C \gg C_{IN}$, or if they are comparable, pole and zero are sufficiently close to compensate each other. In addition to that, C_C also adds a closed-loop pole at $f_P = \frac{1}{2\pi C_C R_F}$, helpful for noise limitation, especially for maximum gain (R_F=358.4 kΩ).

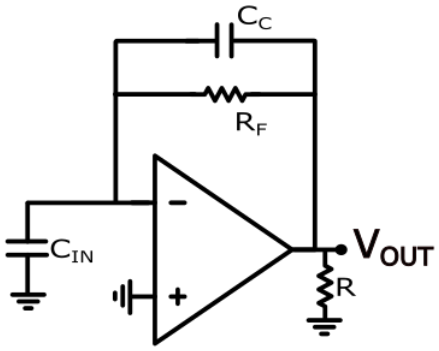


Figure 3.8: Simplified schematic of the TIA

The circuit for the computation of the loop gain around this first amplifier is reported in Fig. 3.8, whereas the related Bode plots and fundamental parameters are shown in Fig. 3.9 and Tab. 3.4. It is possible to appreciate that, for increasing values of R_F, both the pole and the zero highlighted in eq. 3.8 move to lower frequency, while the pair of complex conjugate poles remains at the same frequency as in the open-loop gain.

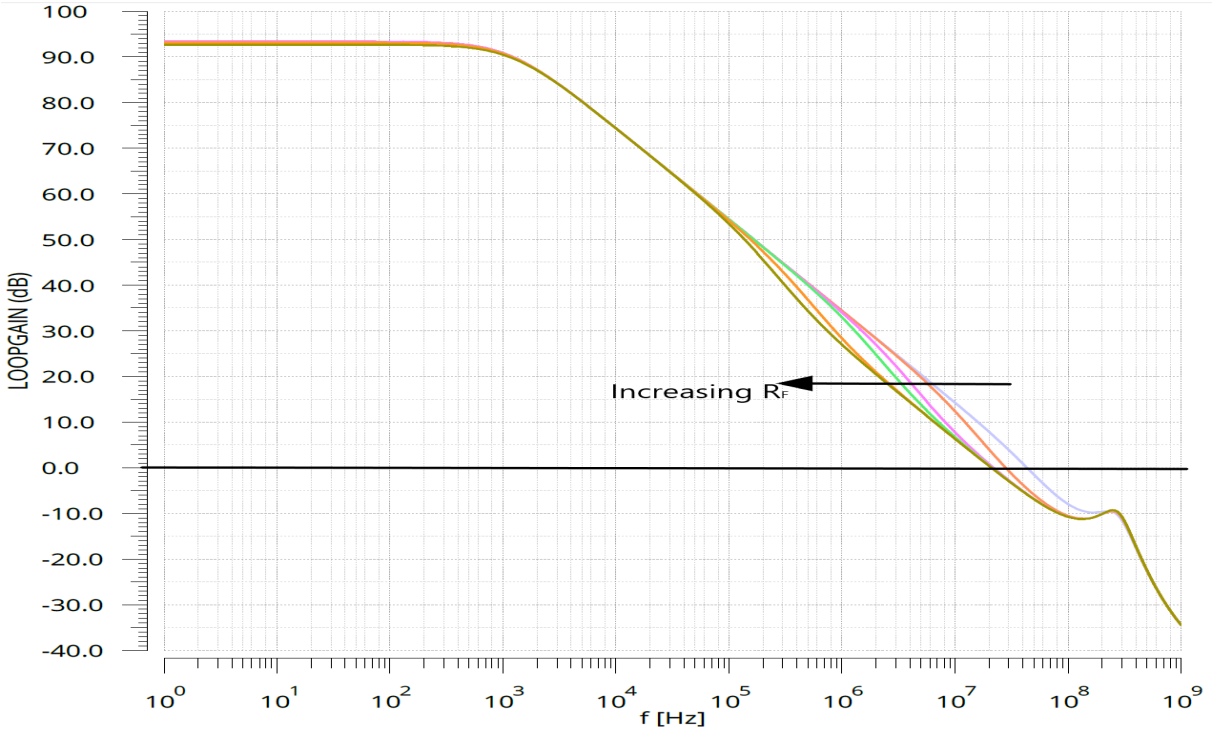


Figure 3.9: Bode plot of the loop gain around the first TIA for the six different configuration of the resistive network

R_F [kΩ]	R [kΩ]	f_{0dB} [MHz]	Phase Margin
1.4	800	43.5	70.7°
5.6	800	28.2	69.5°
22.4	800	22	81.9°
44.8	400	21.3	86.8°
179.2	400	21.1	91°
358.4	200	21.1	91.7°

Table 3.4: Significant values for the loop gain around the first amplifier for different values of R_F and R

Noise analysis

The target of the design of the amplifier, for what concerns noise, was to keep it negligible with respect to the shot noise of the photodiode, reported in Eq. 3.1. This is the main justification in the choice of both the size and the transconductance of the differential pair:

- With respect to **white noise**, the expression of the input referred voltage spectral density can be written as:

$$S_{V_{IN1}} = \frac{8kT\gamma}{g_{m1}} \cdot \left(1 + \frac{g_{m3}}{g_{m1}}\right) \tag{3.9}$$

  with k being the Boltzmann's constant and $\gamma = \frac{2}{3}$. Beware that the pair $M_{A1,2}$, being used in cascode configuration, ideally does not add any noise.

- With respect to **1/f (flicker) noise**, the so-called *Tsividis' formula* [23] states that, due to charge trapping effects averaging out, the input referred spectral density is inversely proportional to the input transistor area $W \cdot L$.

It is thus clear that increasing W of the input transistors reduces both white and 1/f noise. The simulation proves that this amplifier has an input referred voltage spectral density of $S_{V_{IN}} = 6.4\,\frac{nV}{\sqrt{Hz}}$, and a noise corner frequency of $f_C \approx 17\,kHz$. Simulation results are reported in Fig. 3.10.

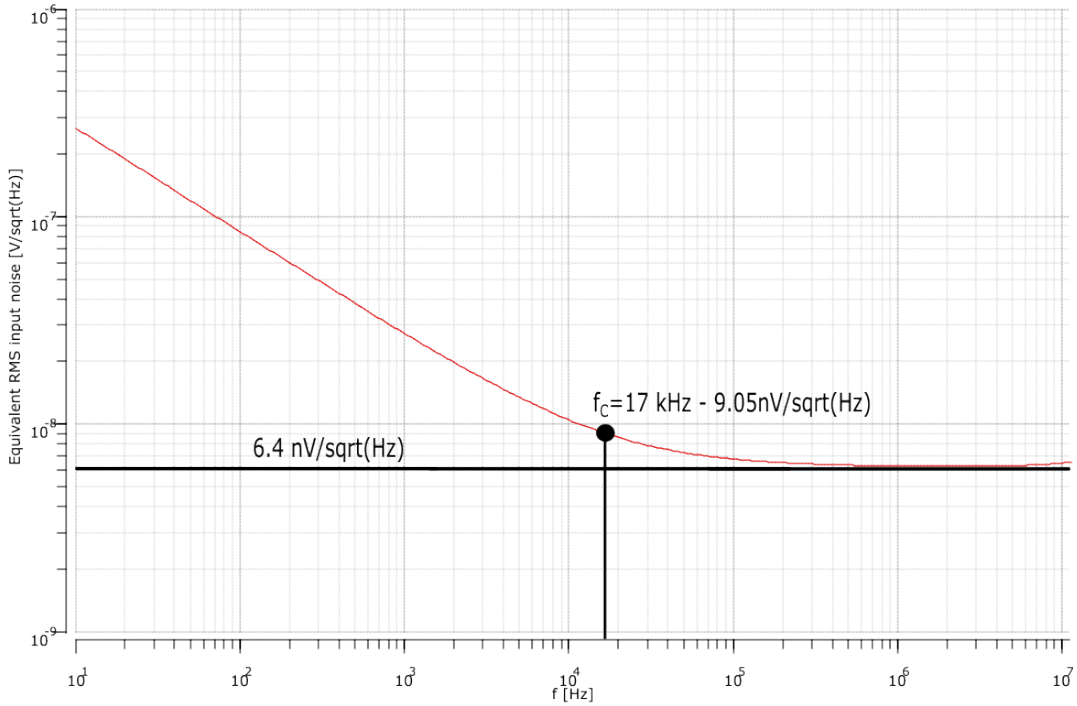


Figure 3.10: Input referred equivalent voltage spectral density of the first amplifier

3.2. Gated Integrator

3.2.1. OTA

The topology chosen for the OTA powering the gated integrator is the same as the one adopted for the first OpAmp of the stage, the only modifications being made in the parameters of the components, reported in Fig. 3.11 and Tab. 3.5.

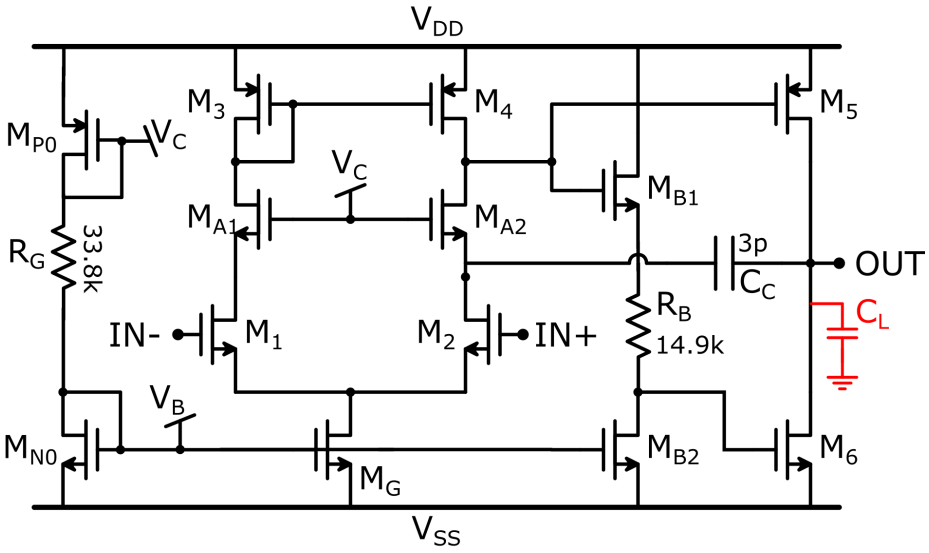


Figure 3.11: Schematic of the OTA and the polarization network for the amplifier of the Gated Integrator

Device	V_T [V]	V_{OV} [V]	V_{DS} [V]	I_{DS} [μA]	W [μm]	L [μm]	g_m [μS]	r_0 [kΩ]
M_{n0}	0.53	0.15	0.68	50	34	1.2	560	600
M_{p0}	0.72	0.20	0.92	50	60	1.2	450	450
M_g	0.53	0.15	0.54	150	110	1.3	1680	160
$M_{1,2}$	0.69	0.31	0.73	75	25	2.4	440	660
$M_{3,4}$	0.72	0.15	0.87	75	140	1.2	820	290
$M_{A1,A2}$	0.88	0.12	1.05	75	35	0.6	970	190
M_{B1}	0.88	0.15	1.90	50	33	1.2	560	1480
M_{B2}	0.53	0.15	0.67	50	33	1.2	560	590
M_5	0.72	0.15	1.65	150	250	1	1670	160
M_6	0.53	0.15	1.65	150	150	1.75	1700	360

Table 3.5: Fundamental parameters of all the MOS devices in the schematic of the OTA

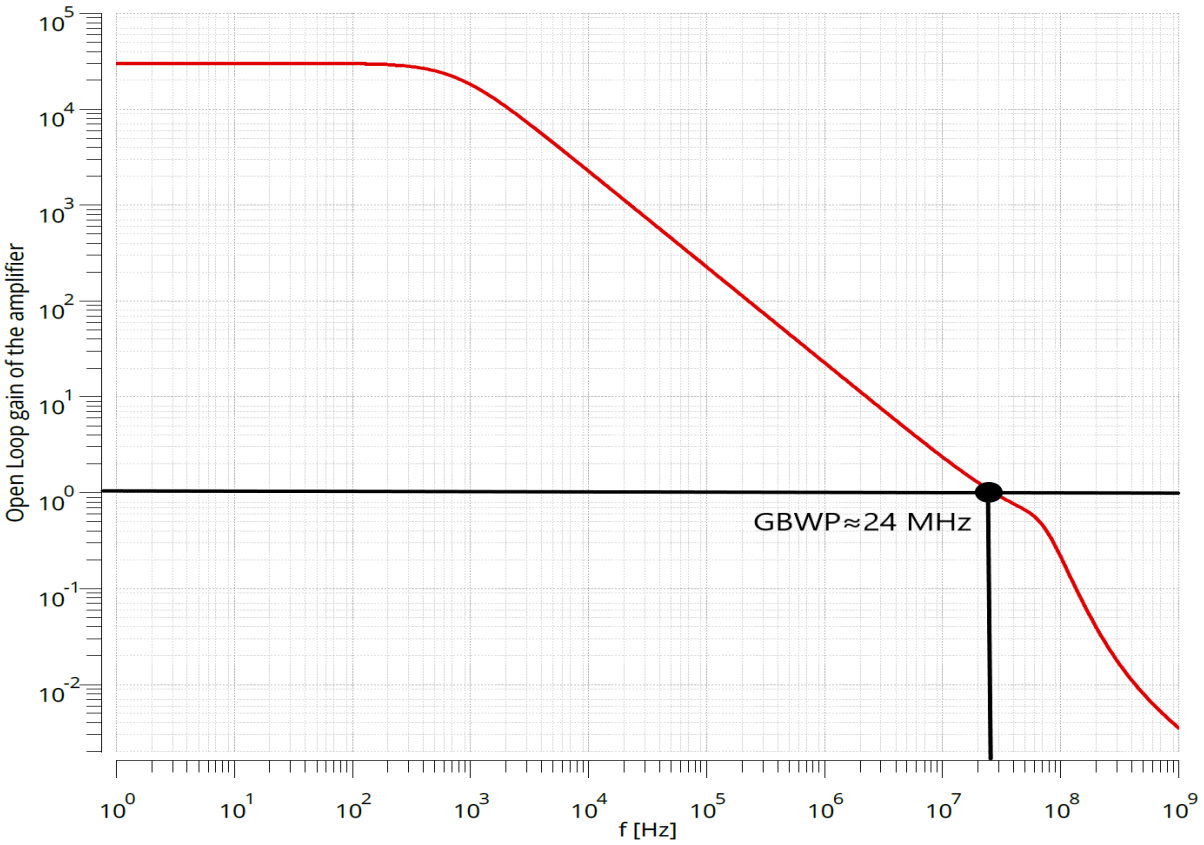


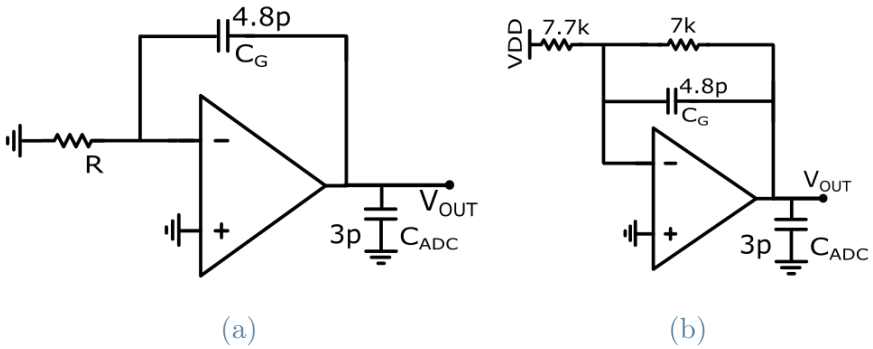
Figure 3.12: Open-loop gain of the amplifier powering the Gated Integrator

In this case power consumption is kept lower, down to P_D=1.3 mW, with choices for bias currents being due to slew rate requirements (sec. 3.2.2). With respect to the amplifier in sec. 3.1.3 the output stage current is way smaller; however, the two transistors of the output stage have comparable sizes in order to provide, here, a sufficiently small V_{OV}, thus allowing for a larger voltage output swing.

Open-loop gain and closed-loop stability analysis

The open-loop gain can be computed using the very same formulas adopted in sec. 3.1.3. Considering a load capacitance of C_L ≈8 pF (C_{ADC}+C_G), the resulting characteristic values of the open-loop gain are G(0)≈ 89.5 dB, f_{LFP} ≈ 770 Hz, GBWP≈23 MHz, f_Z ≈ 103 MHz, f_0 ≈ 100 MHz and Q≈0.18, meaning that the poles, due to the large value of C_L, will be real and no resonance peak can be observed in Fig. 3.12.

Regarding closed-loop gain and stability, the gated integrator may appear with two different configurations (Fig. 3.13), depending whether the stage is actually integrating the signal or it is resetting the capacitance C_G.



(a) (b)

Figure 3.13: Two configurations of the gated integrator: integration of photodiode current (a) and reset of C_G (b)

As a consequence, two different loop gains should be evaluated, with particular care for the integration phase. Simulation results are reported in Fig. 3.14 and 3.15.

Looking at Fig. 3.15, the loop gain seems going to 0 for lower frequencies: this is not a surprise, having a feedback network made just with a capacitor, which behaves as an open circuit at DC. However, the loop is active during reset phase, and maintains the virtual ground at "-" node of the OpAmp. When the switches open to start the integration of the signal, the voltage across C_G is fixed, and can only be modified by the current coming from the resistance R.

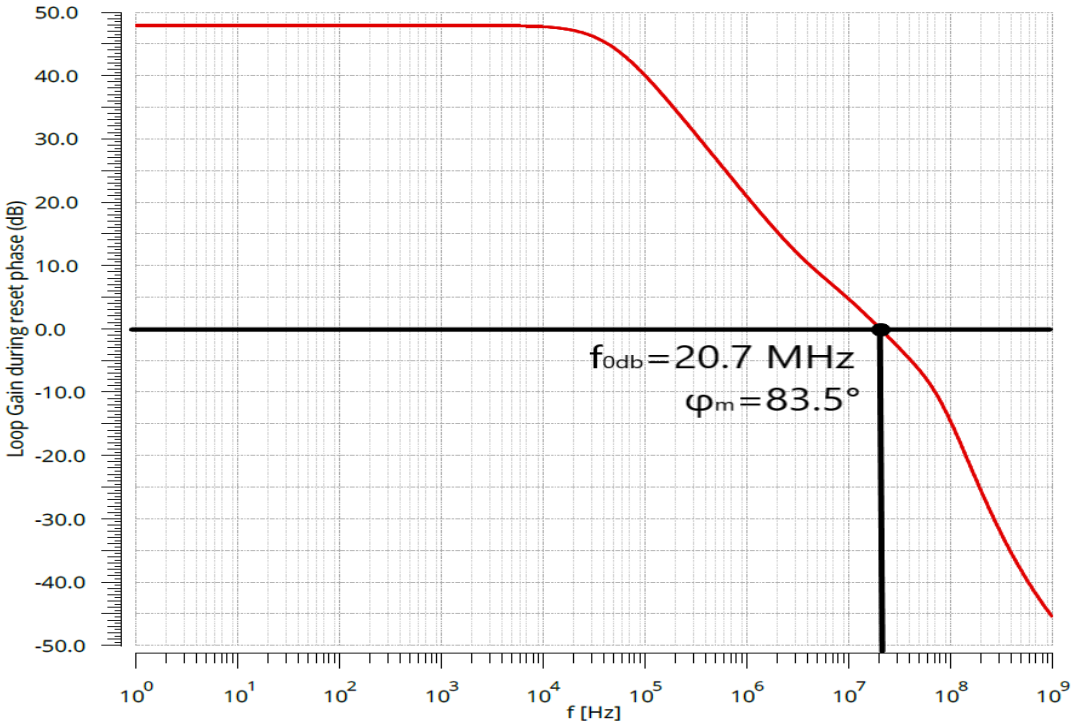


Figure 3.14: Loop gain of the Gated Integrator during reset phase

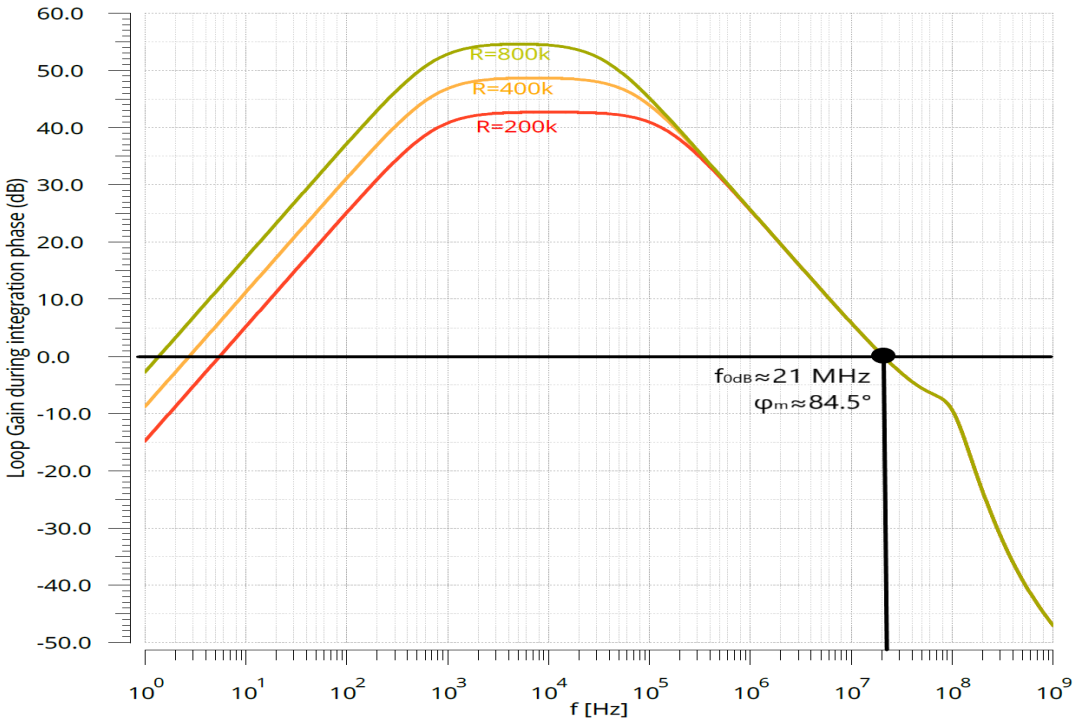


Figure 3.15: Loop gain of the Gated Integrator during integration phase

Noise analysis of the TIA

The same considerations done in sec. 3.1.3 can be made for the amplifier of the GI. However, the noise of this stage is less relevant than that of the first amplifier, and a more relaxed design can be adopted when sizing the bias currents and the dimensions of the transistors in the differential pairs. Recalling eq. 3.9, it is possible to estimate the input referred voltage white noise as $S_{V_{IN2}}$=13.66 $\frac{nV}{\sqrt{Hz}}$, with a noise corner frequency at 20 kHz. The plot of the spectral density is reported in Fig. 3.16.

3.2.2. Sampling and reset mechanism

The bias currents of differential and output stages are justified by the slew-rate requirements. In fact, during the reset phase the amplifier should be able to discharge the Miller compensation capacitance C_C and the load capacitance of the ADC (specified in the datasheet as C_{ADC}=3 pF [24]) within $\frac{1}{2}$ clock period, corresponding to ≈450 ns. The *internal* slew rate limit is set by the total current of the differential stage to:

$$SR_{int} = \frac{2I_{M1}}{C_C} = 50\,\frac{V}{\mu S} \tag{3.10}$$

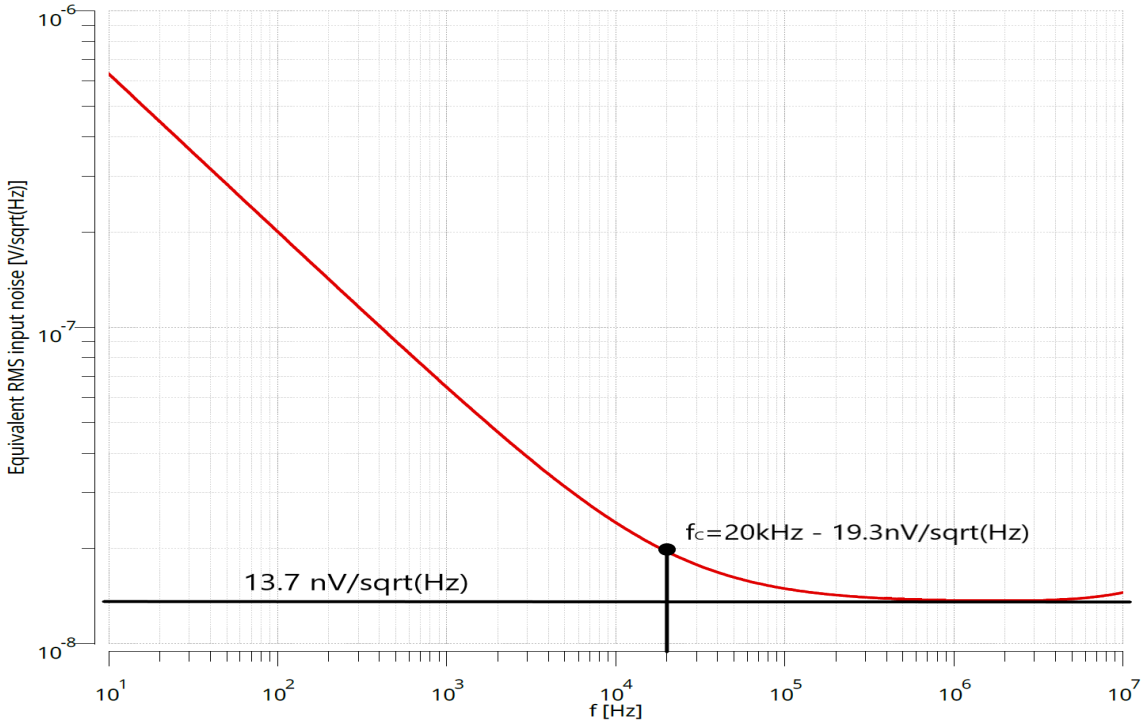


Figure 3.16: Input referred equivalent voltage spectral density of the amplifier powering the gated integrator

which allows a sufficiently fast discharge of C_C. A similar consideration applies for the discharge of C_L, corresponding here to C_{ADC}. Also in this case, the bias current of M_5 and M_6 is sufficient to provide the necessary voltage swing (up to ΔV_{OUT}=3.15 V) at the output node within the required time. The reset action is implemented by means of a couple of resistors (Fig. 3.13): when the switches close, V_{OUT} undergoes an exponential transition towards the asymptotic value $VDD \cdot \frac{7\,k\Omega}{7.7\,k\Omega} = -1.5\,V$ with a time constant $\tau = C_G \cdot 7\,k\Omega = 33.6$ ns. The complete reset phase lasts 0.5 clock cycles, corresponding to ≈450 ns: it is more than $13\,\tau$, so the transient can well be considered over when the switches open again to start a new integration.

3.3. Signal to Noise ratio of the stage

It might be interesting to compute the *rms* value of the voltage noise affecting the sample taken by the ADC at the end of the integration. To do so, all the white noise sources are reported in Fig. 3.17.

Considering all the noise sources, the current spectral density S_I being integrated on C_G

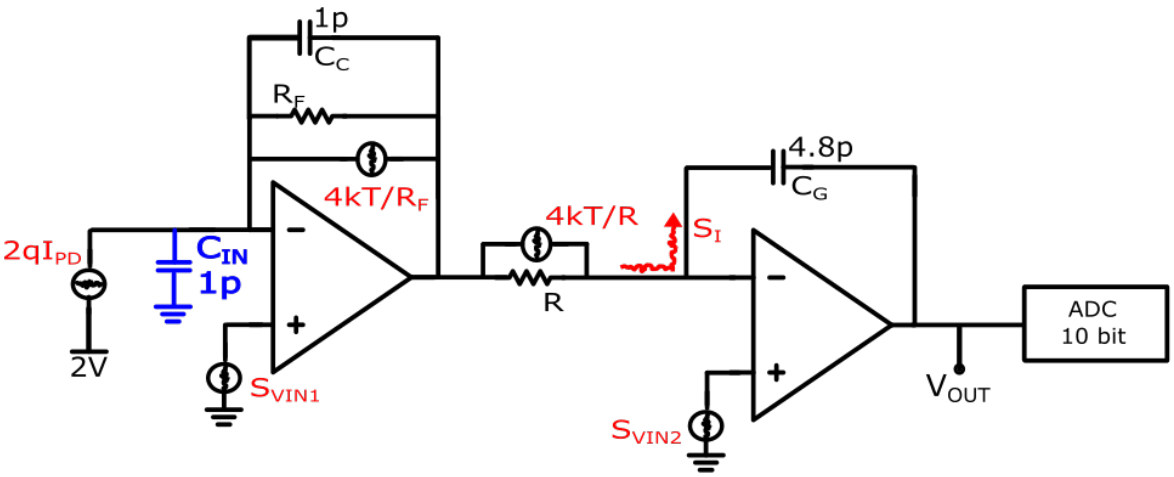


Figure 3.17: Schematic of the analog front-end with all the noise sources highlighted

can be written, for frequency lower than $f_P = \frac{1}{2\pi C_C R_F}$ as:

$$\begin{aligned} S_I &= 2qI_{PD}(\frac{R_F}{R})^2 + \frac{4kT}{R_F}(\frac{R_F}{R})^2 + S_{V_{IN1}} \cdot (2\pi f \cdot C_{IN})^2 \cdot (\frac{R_F}{R})^2 + \frac{4kT}{R} + \frac{S_{V_{IN2}}}{R^2} \\ &= \frac{1}{R^2} \cdot \left[2qI_{PD}R_F^2 + 4kTR_F + S_{V_{IN1}} \cdot (2\pi f \cdot C_{IN})^2 R_F^2 + 4kTR + S_{V_{IN2}}\right] \end{aligned} \tag{3.11}$$

which clearly highlights that, the larger R, the smaller the value of S_I. A couple of remarks could be made with respect to the noise of the two amplifiers:

- The voltage noise of the first amplifier gives rise to the current noise $S_{V_{IN1}} \cdot (2\pi f \cdot C_{IN})^2$. Such noise is obviously nil at DC, and undergoes the same transfer function as $2qI_{PD}$, starting from the pole set by $R_F C_C$. It is interesting to observe the ratio between the two noise contributions at the frequency of the pole for different values

G_{IN}	$I_{PD_{MAX}}$[µA]	$I_{PD_{min}}$[µA]	R_F[kΩ]	$f_P = \frac{1}{2\pi C_C R_F}$[MHz]	$\frac{2qI_{PD}^{min}}{S_{V_{IN1}} \cdot (2\pi f_P C_C)^2}$
1	850	212.5	1.4	114	3
2	212.5	53.12	5.6	28.4	12
3	53.12	13.28	22.4	7.1	48
4	13.28	3.32	44.8	3.5	48
5	3.32	0.83	179.2	0.89	192
6	0.83	0.15 (Dark current)	358.4	0.45	136

Table 3.6: Ratios between photodiode and OpAmp noise in the transimpedance amplifier for different values of G_{IN}

of G_{IN}, reported in Tab. 3.6.This proves that the noise from the OpAmp is always negligible compared to shot noise associated with the optical signal (please note that for G1 and G2 f_P is beyond the f_{0dB} of the stage).

- The voltage noise of the second amplifier gives rise to the current noise $\frac{S_{V_{IN2}}}{R^2}$. Since the ratio $\frac{4kTR}{S_{V_{IN2}}} \gg 1$ for whatever value of R, also this contribution is negligible.

As a result, it is possible to simplify the total current noise injected on C_G as:

$$S_I = \frac{1}{R^2} \cdot (2qI_{PD}R_F^2 + 4kTR_F + 4kTR) \tag{3.12}$$

A nice feature is that, at least for R_F=358.4 kΩ, i.e. for the most important operating region of the system (minimum optical power on the photodiode), where the highest precision is required, the shot noise associated to the signal is always larger than the white noise associated to the electronic components of the acquisition chain.

$\mathbf{G_{IN}}$	$\mathbf{I_{PD_{MAX}}}$[µA]	$\mathbf{R_F}$[kΩ]	R[kΩ]	$\frac{2qI_{PD}^{MAX}R_F^2}{4kTR_F}$	$\frac{2qI_{PD}^{MAX}R_F^2}{4kTR}$
1	850	1.4	800	23	0.04
2	212.5	5.6	800	23	0.16
3	53.12	22.4	800	23	0.64
4	13.28	44.8	400	11.5	1.35
5	3.32	179.2	400	11.5	5.1
6	0.83	358.4	200	5.7	10.3

Table 3.7: Ratios between shot noise associated to the signal and noise sources associated to the electronics

Coming to the signal to noise ratio, the weighting function of the gated integrator can be written, in time domain, as

$$w_{GI}(\alpha) = \frac{1}{C_G} \cdot rect(\frac{\alpha}{T_G}) \tag{3.13}$$

Its auto-correlation function is defined as

$$k_{ww}(\alpha) = \int_{-\infty}^{+\infty} w(\alpha) \cdot w(t-\alpha)d\alpha = \frac{T_G}{C_G^2} \cdot tri(\frac{\alpha}{T_G}) \tag{3.14}$$

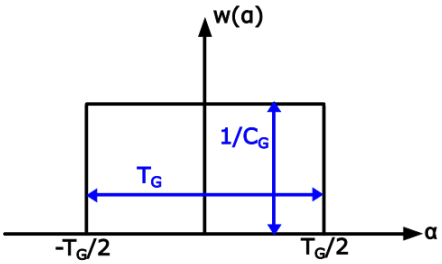


Figure 3.18: Weighting function of a gated integrator

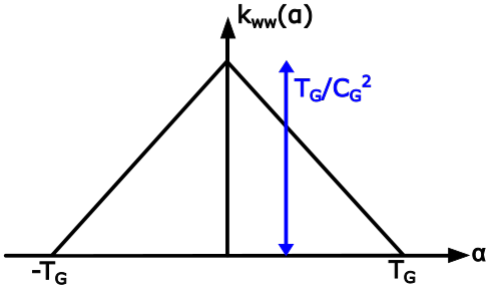


Figure 3.19: Autocorrelation function of the gated integrator

Finally, exploiting the *Parseval's theorem*, it is possible to write the output rms noise as

$$\sqrt{\sigma^2_{OUT}} = \sqrt{\int_{-\infty}^{+\infty} S_I(f) \cdot |W(f)|^2 df} = \sqrt{\int_{-\infty}^{+\infty} R_{xx}(\alpha) \cdot k_{ww}(\alpha) d\alpha} \tag{3.15}$$

where $R_{xx}(\alpha) = S_I(0) \cdot \delta(\alpha)$ is the auto-correlation of the current noise spectral density[2] injected into C_G (which is ideally constant, at least for a wide range of frequency, larger than the one of interest) and |W(f)| is the module of the Fourier-transform of the gated integrator's weighting function. That being said, the expression for the rms output noise can be written in a very simplified way as

$$\sqrt{\sigma^2_{OUT}} = \sqrt{S_I(0) \cdot k_{ww}(0)} = \sqrt{S_I(0) \cdot \frac{T_G}{C_G^2}} \tag{3.16}$$

with values of $\sqrt{\sigma^2_{OUT}}$ ranging from 67 μV_{rms} for the lowest gain of the stage to 475 μV_{rms} for the largest gain, the one with I_{PD}^{MAX}=830 nA, R_F=358.4 kΩ and R=200 kΩ. It is worth pointing out that the gated integrator implements, with respect to noise, the same filtering

[2]Beware that in these computations S_I is the **bilateral** current spectral density. The values derived from eq. 3.12 here should be divided by a factor 2

action as an RC low-pass filter with RC=2T$_G$ ≈19 μs: in the assumption of C=C$_G$, a resistor R≈8 MΩ would be needed to match the gated integrator with a passive RC network!

As a final contribution, the switching noise of the reset resistor on C_G should be considered, too. It is well known that its rms value is independent from the resistor size and it is only related to the value of C_G:

$$\sqrt{\sigma^2_{OUT,switch}} = \frac{kT}{C_G} = 29.4\,\mu V_{rms} \tag{3.17}$$

The two contributions, however, should now be compared to the quantization noise of the ADC, defined as:

$$\epsilon_q^2 = \frac{LSB^2}{12} = \frac{(\frac{3.3V}{2^{10}})^2}{12} = 930\,\mu V_{rms} \tag{3.18}$$

Since the ADC only has 10 bits, the resulting quantization noise is pretty high, always dominant over the noise from the analog chain. As a result, in the worst case the total output noise sums up to

$$\sqrt{S_I(0)\cdot\frac{T_G}{C_G^2} + (\frac{kT}{C_G})^2 + \epsilon_q^2} = \sqrt{(475\,\mu V_{rms})^2 + (29.4\,\mu V_{rms})^2 + (930\,\mu V_{rms})^2} = 1.04\,mV_{rms}$$

which is still well below 1 LSB.

At last, some considerations should be made on the signal. Let us consider the waveform of the current in the photodiode in the assumption of having just one dithering signal. It would appear like a square wave, reported in Fig. 3.20.

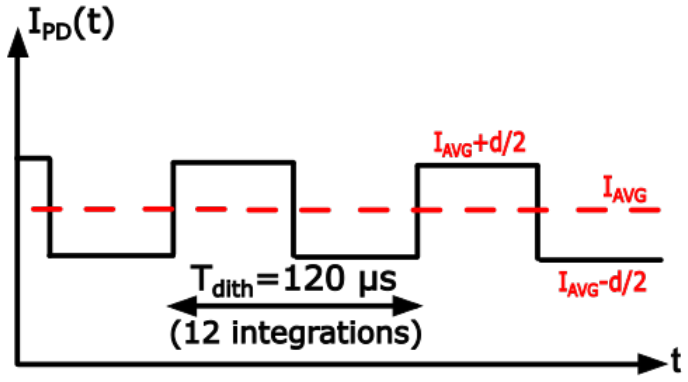


Figure 3.20: Simplified waveform of the current in the photodiode

Indeed, if the extraction of the dithering signal from the 12 samples had no digital part,

the Signal to Noise Ratio (SNR), and consequently the minimum dithering amplitude could be easily computed as

$$\frac{S}{N} = \frac{\frac{d}{2} \cdot \frac{R_F}{R} \cdot \frac{T_G}{C_G}}{\sqrt{S_I(0) \cdot \frac{T_G}{C_G^2} + (\frac{kT}{C_G})^2}} \cdot \sqrt{12} \tag{3.19}$$

with $\frac{S}{N}$=1 being obtained, in case of maximum gain, with d≈77 pA.

However, the presence of some quantization has to be taken into account: in order for the digital chain to extract a non-nil dithering amplitude when demodulating the ADC output, it is necessary that the samples representing the values $I_{AVG} + \frac{d}{2}$ and $I_{AVG} - \frac{d}{2}$ differ by at least 1 LSB. This is like asking that the amplitude of the dithering modulation, in terms of photodiode current, is ≥1 LSB. The condition to be satisfied is

$$d \geq 1\, LSB \cdot \frac{C_G}{\frac{R_F}{R} \cdot T_G} \tag{3.20}$$

and it is more stringent than the one on $\frac{S}{N}$: the minimum value for the dithering amplitude ranges from 900 pA (equivalent to -59.7 dBm of modulation on light intensity) for the maximum gain region up to 920 nA (-29.6 dBm) when the gain of the stage is the minimum one, in order to handle large current/light intensity.

4 | Digital circuit

Introduction

The major update brought to this circuit with respect to its predecessors is the implementation at digital level of many of the operations that were previously performed by analog circuits, including the likes of signal demodulation and dithering extraction, automatic adjustment of the gain G_{IN} of the analog front-end and eventually the management of system saturation and reset. The motivations behind this choice are:

- Digital systems, in opposition to analog ones, follow Moore's law, meaning that they can be scaled in size while preserving the overall performance. As it will be shown, the goal of controlling a 15 MZIs mesh is barely satisfied with the adopted technology (AMS C35B4, with a feature size of 0.35 μm), thus suggesting that a digital approach becomes a real game-changer when moving to smaller technology nodes;
- The speed of the digital system is determined by the clock frequency. In this project it is set at 1.1 MHz by the ADC timings, but it could be increased for faster elaboration of the dithering information - the ultimate limit being set by the "thermal" bandwidth of the heater, estimated at $\approx$1 MHz;
- Many parameters that regulate the operation of the system (thresholds, dithering amplitude, bandwidth...) are set externally, according to the requirements of each case; at the same time, it is easy to extract data from the system (photodiode current, heater control voltage...). These operations will be performed with two shift registers, connected serially to the external world, thus requiring only two pads. It will be also possible to deactivate the control-loop in order to check the open-loop operation of the system and even to externally set all the control voltages on the heaters, something that could not be done in the previous fully-analog designs, as well as storing in the register a particular state of the system that could be recalled in the future.

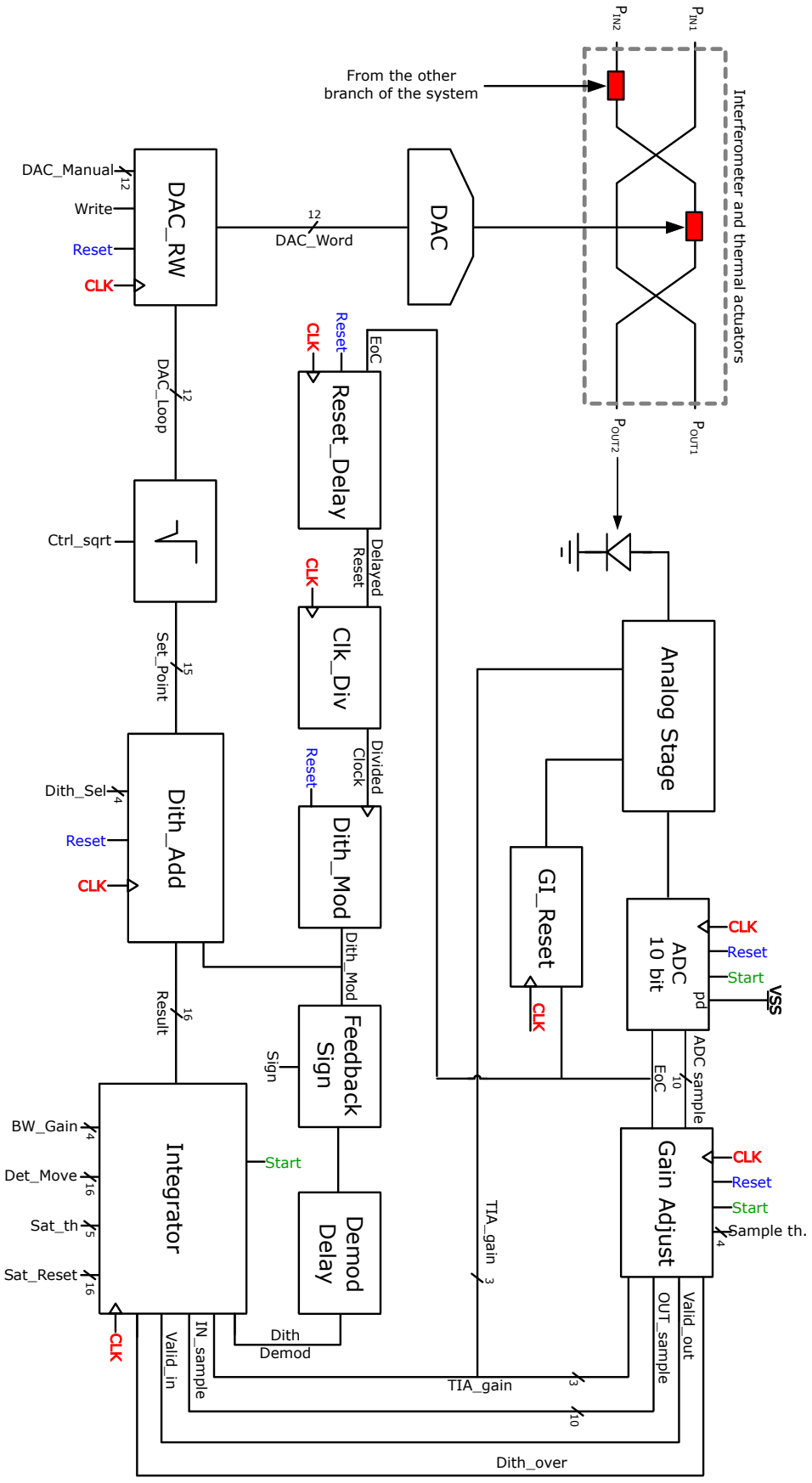


Figure 4.1: Scheme of the full control system. The second branch of the digital circuit is identical to the reported one, departing after the *Gain_ Adjust* module

Reported in Fig. 4.1 is the full architecture of a **single** branch of the digital system. It should be recalled that each MZI is controlled by two heaters: after the *Gain Adjust* block, the channel splits into two identical paths that lead to the two actuators.

The core of the digital circuit is constituted by: an ADC, delivered by AMS; a *Gain Adjust* block that manages the operation of the analog stage and elaborates the sample to be fed to the integrator; the integrator, which store and determines the working point of the actuator. These blocks are followed by the chain that allows to add the dithering modulation, make the square root and the DAC, with the option (with DAC_RW) of an external setting of the digital word that the DAC (which is being developed in another thesis project alongside the circuit to drive the thermal actuators) converts into the heater voltage. On top of that, particular care had to be put in the description of the blocks that allow a precise timing of the dithering application and the demodulation process. All the blocks will now be reviewed in detail.

All the cells that constitute the circuit belong to the technology AMS C35B4 (feature size 0.35μm, 4 metal layers), from the CORELIBD library, dedicated to logic gates. Each block of the system was described in VHDL. The Cadénce suite, used for the design of the whole chip, provides the designer with two useful softwares, *Genus* and *Innovus* [25, 26]: the former allows to synthesize a schematic from the VHDL code, using cells belonging to user-defined libraries (CORELIBD in this case [27]); the latter is meant to generate the layout of the circuit, starting from its Verilog description, created by Genus. Both softwares allow the designer to set timing, power and area constraints to be respected in the choice of the standard cells during the synthesis. Finally, schematic and layout can be exported to *Virtuoso* simulation and integration in the overall architecture of the chip.

4.1. ADC and Reset of the Gated Integrator

4.1.1. Converter

The very first component that connects the analog front-end to the digital circuit is the successive approximation ADC10A, given as an Analog Standard Cell by AMS, complete of schematic and layout down to transistor level.

Its pins are shown in Fig. 4.2: as suggested in the datasheet [24], analog and digital power supplies are both connected to $\pm 1.65\,V$, as well as the voltage references (VRP, VRN) that determine the voltage range to be mapped with the ADC's 10 bits and set the LSB at $LSB = \frac{3.3\,V}{2^{10}} \approx 3.23\,mV$. The *pd* (*power down*) is always kept low: the ADC is just turned on/off with *start*, which is driven externally. This last choice implies that, once

start has gone high (Fig. 4.3), the ADC will continuously make conversions and produce a digital output: it is the *Gain Adjust*'s task to decide what to do with the sample.

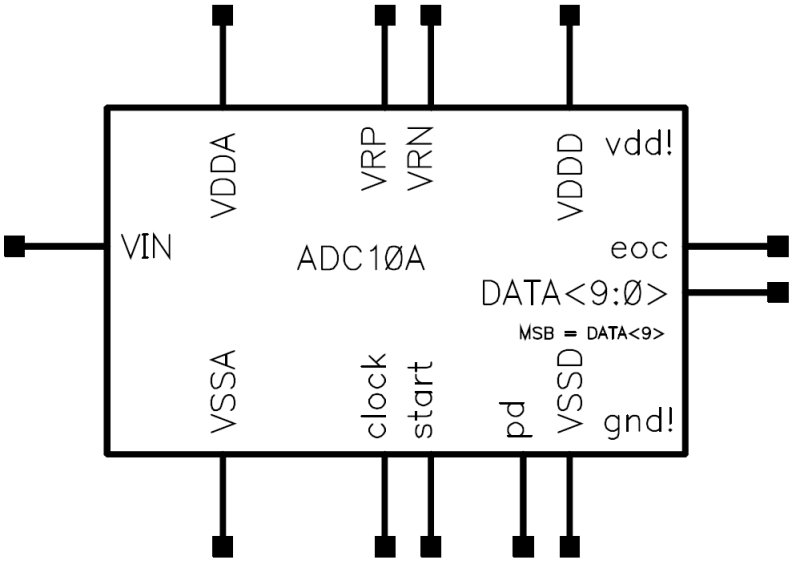


Figure 4.2: Symbol of the ADC complete of its pins

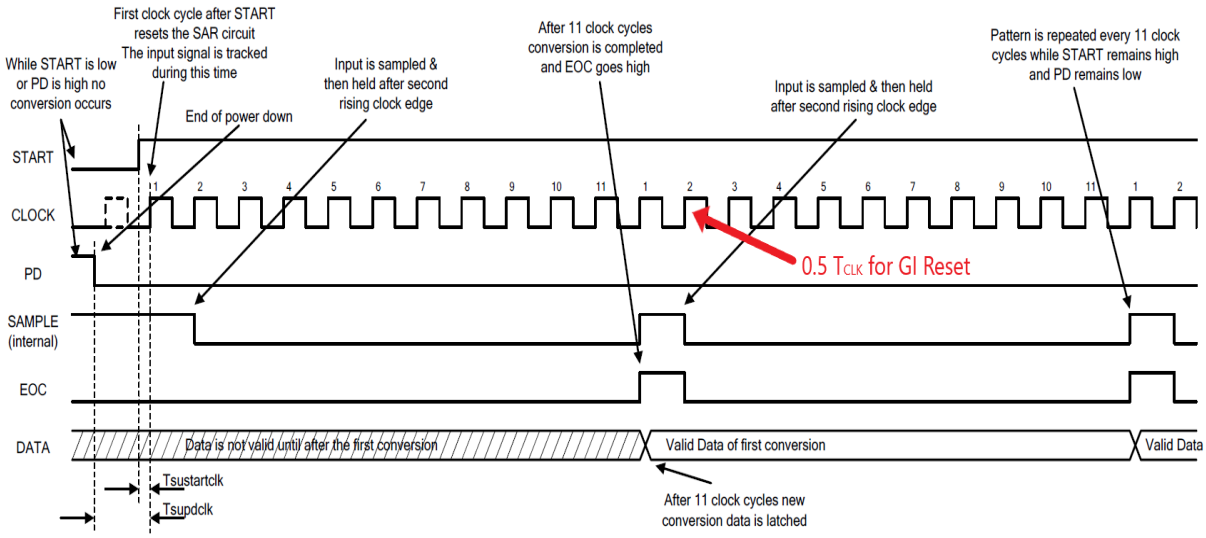


Figure 4.3: Timing of the ADC when working in continuous conversion mode

The clock frequency of the component is 1.1 MHz, which has also been chosen as the clock frequency of the whole circuit. The ADC needs 11 clock cycles to determine its output digital word: the first cycle is used for sampling and holding of the analog signal, the remaining 10 to determine each bit of the conversion (Fig. 4.3). The resulting sampling time is $T_s = \frac{11}{1.1\,MHz} = 10\,\mu s$, meaning that each dithering period is sampled 12 times: as

shown in Chapter 3 this is beneficial for the Signal-to-Noise Ratio, but there will be an impact on the number of bits required in the integrator.

4.1.2. Reset of the gated integrator

Waveforms reported in Fig. 4.3 suggest that the command for the switches that periodically activate the reset of the gated integrator could be triggered by the *EoC* signal produced by the ADC, which is repeated every 10 μs. In the implementation of this function, there are 3 things to take into account:

- The reset should happen right at the beginning of the analog integration, or, said it in another way, just after the S&H operation;
- The switches should be closed for the shortest possible time, which corresponds, using a single clock frequency, to $0.5 \cdot T_{CLK}$, equivalent to $T_{RST} = \frac{1}{2 \cdot f_{CLK}} \approx 450$ ns;
- It is crucial that the reset operation never anticipates the input holding that happens on the second clock rising edge, nor that they happen simultaneously.

To satisfy the first and the third requirement, a delay cell (DLY4X1 from CORELIBD) is introduced between the logic that activates the reset (*GI_Reset*) and the switches in the analog stage. As a result, the S&H operation anticipates by ≈10 ns the reset of the integration capacitance.

Clearly, the circuit that produces an output that lasts only a fraction of the clock period needs some asynchronous logic, as it is shown in Fig. 4.4: triggering the *flip-flop* on the falling edge of the clock allows to create a copy of *EoC* delayed by just $0.5 \cdot T_{CLK}$.

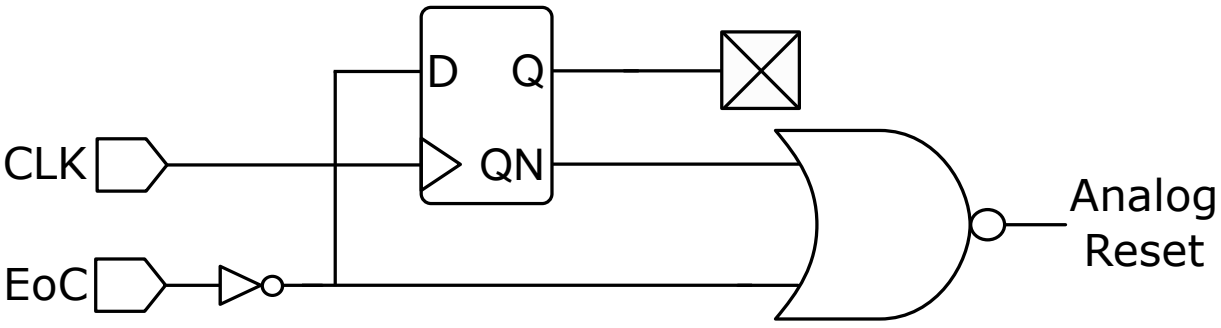


Figure 4.4: Circuit for the activation of the reset on the falling edge of *EoC*

4.2. Automatic Variable Gain

As highlighted in Chapter 4, the analog stage has to deal with a wide range of currents (from 850 μA when 1 mW is impinging on the photodiode down to 150 nA of dark current): a variable gain (G_{IN}) was introduced in the stage in order to describe the working points of the device with the proper resolution and to extract a dithering modulation that must be sufficiently small so as not to impair the locking of the optical device to its minimum.

The adjustment of G_{IN} is done automatically with the *Gain Adjust*, which is reported in Fig. 4.5. The component, which is shared between the two branches of the channel, implements several functionalities:

- Determines the 3 bits digital word *TIA_gain* that controls the value of G_{IN} in the analog stage;
- Initializes G_{IN} to the maximum possible value (*TIA_gain*="101") when *start* is low. The choice is motivated by the fact that, in the lucky case the MZI is already working in a minimum of its transfer function at the beginning of the operation, G_{IN} would be set to the proper value;
- Provides the integrator with the information needed to correctly weigh the sample, as well as the single bit that signals when a full dithering period has been completed (12 samples);
- When *Reset* (which is an external command, with a dedicated pad) is high, sets to '0' all the bits of *Out_sample*, fed to the integrator: as a consequence, the working point of the system (output of the integrator) will not change. This is one way the user can deactivate the control loop, and eventually, as it will be showed in the following, manually set a working point for each DAC. Obviously, when *Reset* is low *ADC_sample* is simply passed to *Out_sample*.

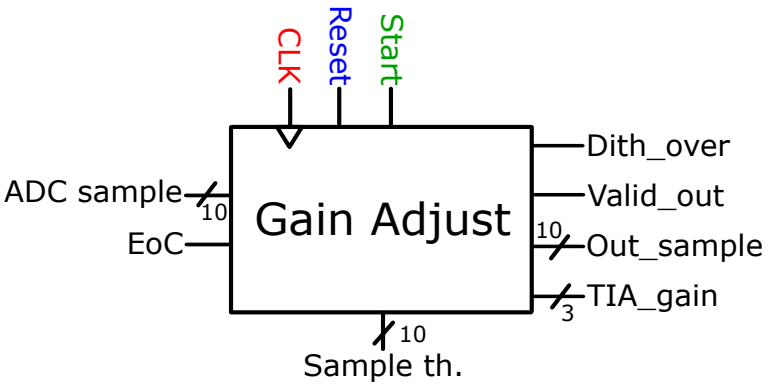


Figure 4.5: Symbol of *Gain Adjust* complete of its pins

As shown in Chapter 3, Tab. 3.1, the thresholds that determine a change of G_{IN} are set on the values of the current in the photodiode, in a manner such that the relation $I_{PD}^{MAX} = 4 \cdot I_{PD}^{min}$ is always true. The fact that also G_{IN} is progressively scaled by a factor 4 allows to write $I_{PD}^{MAX}|_{G_{IN}=i} = I_{PD}^{min}|_{G_{IN}=i+1}$, meaning that the voltage values at the output of the analog stage corresponding to the thresholds are the same for whatever value of G_{IN}. These values can be reported to the digital ADC sample as:

$$\begin{aligned} ADC_{th}^{MAX} &= (0.15\,V + I_{PD}^{MAX} \cdot \frac{R_F}{R} \cdot \frac{T_G}{C_G}) \cdot \frac{2^{10}}{3.3\,V} \approx 1.48\,V \\ ADC_{th}^{min} &= (0.15\,V + I_{PD}^{min} \cdot \frac{R_F}{R} \cdot \frac{T_G}{C_G}) \cdot \frac{2^{10}}{3.3\,V} \approx -0.76\,V \end{aligned} \tag{4.1}$$

which ideally correspond to the digital values 970/1023 and 277/1023[1]. These two thresholds are reported on *Sample th.*, although they are approximated with a 5 bits word each in order to save some silicon area; it is important to specify that *Sample th.* is tunable and supposed to be set by the user at the beginning of the operation, so as to compensate for any process related non-ideality that could affect the analog stage. The 5 MSBs of the first *ADC sample* of the dithering period are compared with *Sample th.*: if they match *Sample th.*[9:5], *Gain Adjust* moves G_{IN} to a lower value (since *ADC sample* overcame the upper threshold); if they match *Sample th.*[4:0], *Gain Adjust* moves G_{IN} to a higher value (since *ADC sample* overcame the lower threshold). Finally, it must be specified that this evaluation is made only for the first sample of the dithering period: if it fits in the thresholds, also the following 11 samples will be passed on to complete the integration of the dithering period.

Regarding area occupation, estimated with *Genus*, the device occupies $\approx 11'000\,\mu m^2$.

4.3. Integrator

After *Gain Adjust*, the digital circuit splits into two identical paths: each one will demodulate its own dithering signal to drive the respective actuator.

The *Integrator*, represented in Fig. 4.6, is the fundamental component that:

- Performs dithering demodulation and integration, giving to each sample the proper weight and sign according to the selected bandwidth, the gain G_{IN} of the analog stage and the user made choice about the sign of the feedback (i.e. whether to lock

[1]The analog reset of the gated integrator set back the output node to VSS+0.15 V, taking a 150 mV margin to keep the output transistors in saturation

the MZI close to a minimum or a maximum);

- Initializes the working point of the device when the system is turned on (i.e. when *Start* goes high);
- Modifies its output, that ultimately determines the power dissipated by the heater, every time a dithering integration is complete (signaled by *Dith_ Over*).
- Resets the internal signals that determine *Result* and ultimately the working point of the heater whenever the system gets too close to saturation;
- Moves the working point of the system whenever the result of the integration of a full dithering period does not produce any variation, excluding, obviously, the case of the MZI being locked to a minimum of its transfer function.

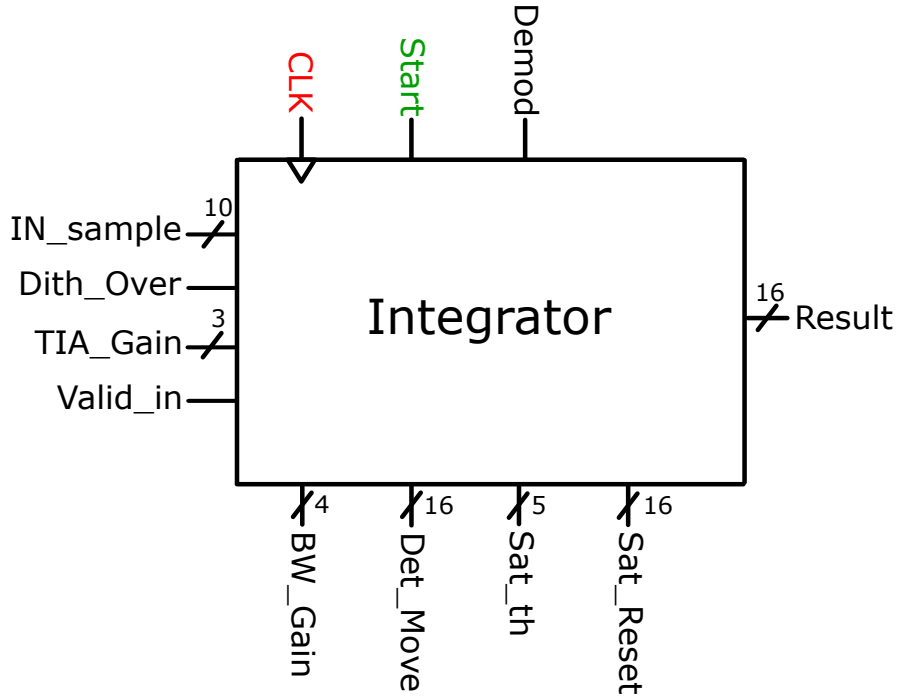


Figure 4.6: Symbol of the integrator complete of its pins

4.3.1. Digital word width

First of all, it could be interesting to justify the number of bits that make up the digital word elaborated by the integrator. In fact, despite only 10 bits sample entering the component and a 16 bits output word[2], the addition/subtraction happening in the integrator involve a 33 bits wide digital word (called *S_ Result*), whose partition is portrayed in Fig. 4.7.

[2]This output word corresponds to the state variable C adopted in Chapter 2

- Each dithering integration involves 12 operations: 6 times *IN_sample* is summed, and 6 times it is subtracted to the value stored in the integrator. As a result, 3 bits to the left of *S_Result*'s MSB and the 3 bits to the right of its LSBs should be allocated for the detection of a possible overflow, which obviously would trigger the reset of the integrator to the value stated by *Sat_Reset*.
- *IN_sample* should be added at a proper position inside *S_Result*. In fact, if for a given value of the analog stage gain G_{IN} the related ADC samples are added to *S_Result* in the portion *S_Result*[i; i-9], it is obvious that, every time G_{IN} is increased by one step (a factor 4), then the bits where *IN_sample* is summed should be shifted twice to the right, on *S_Result*[i-2; i-11]. The ADC, in fact, is describing a region of the MZI's transfer function which is 4 times smaller (i.e. "less significant") with respect to the previous one, as reported in Chapter 3, Fig. 3.3. Since G_{IN} has 6 different values, 5 transitions are possible, meaning that *S_Result* needs at least 20 bits just to manage the variable gain. This is equivalent to say that the resolution of the conversion is raised from the 10 bits of the ADC up to 20 bits.
- Finally, the possibility of tuning the bandwidth of the system announced in Chapter 2 has to be implemented: it is the task of *BW_Gain*. This digital word, externally set according to the requirements of the application, determines a shift to the left of the sample added to *S_Result*, increasing by a factor 2 its weight and eventually the overall bandwidth.

It is important to observe that, in any case, only the 16 MSBs of *S_Result* are available at the output: the reason is that the following block, implementing an approximated version of the square root only needs 16 bits to determine its 12 bits wide output; in case the application does not require a square root operation, *S_Result*'s 12 MSBs are directly fed to the following blocks.

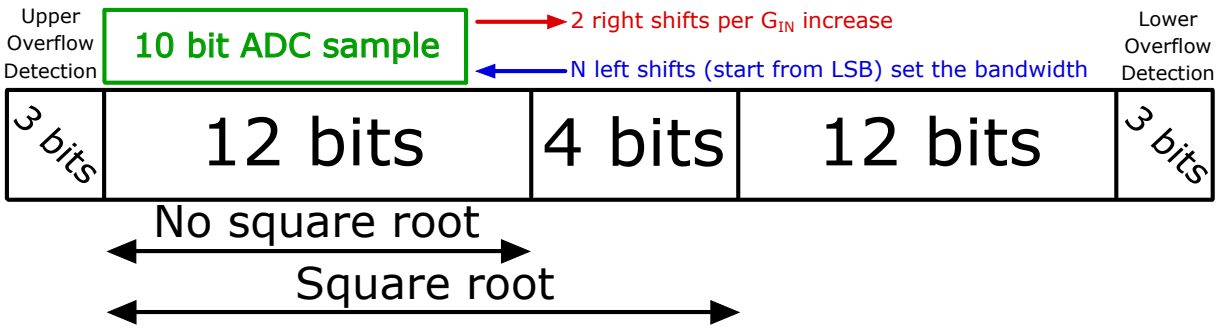


Figure 4.7: Allocation of the 34 bits (28 for *S_Result* and 6 for overflow detection) that constitute the digital word elaborated by the integrator

4.3.2. Deterministic modification of the working point

A limit in the effectiveness of the dithering control strategy, resulting from the adoption of an ADC with limited resolution and thus of a variable gain of the analog stage, arises when the MZIs finds itself operating close to a maximum of its transfer function (Fig. 4.8). The small G_{IN}, necessary to avoid saturation of the analog stage caused by the DC component of $I_{PD}(P_{OUT})$, also applies to the modulation associated with the dithering signal ($I_{PD}^{dith} = S_D \cdot P_d$): combined with the larger LSB of the ADC (which is used to convert a 850 μA wide range of I_{PD} values), the consequence is that there might be a region of the MZI's transfer function where no dithering signal is detected at digital level, thus compromising the control strategy in case the device had to be steered towards a minimum of P_{OUT}, as no modification will be made to the integrator output (the system would be stuck until it spontaneously moves to a working point where dithering can be detected).

The solution is **not** increasing the dithering modulation amplitude, because:

- There will always be some points, centered around the maximum of $P_{OUT}(\phi_H)$, for which the detected dithering amplitude is nil, i.e. those for which the modulation determines two samples which are converted by the ADC with the same digital word.
- An increased dithering amplitude would impair the operation of the system close to the minimum of $P_{OUT}(\phi_H)$, since the modulation of optical power could be large enough to move the P_{OUT} above the targeted rejection ratio.

This issue is solved with a dedicated logic inside the integrator: whenever, after one dithering period, the signal *S_Result* is not modified, the integrator modifies *Result* by adding a quantity *Det_Move*, which is externally defined depending on the application. This algorithm, of course, does not apply when the analog stage is working with G_{IN}^{MAX}: in that case the control loop is actually working to minimize the dithering modulation (the error signal of the system).

4.3.3. Locking to a maximum of P_{OUT}

The drawback of the *Det_Move* solution appears when the system is working so as to try to maximize P_{OUT}. In this case, the system does not stuck when it finds itself in a minimum of P_{OUT}: it is true that the dithering signal in that point is nil, but here it is possible to rely on the noise on ϕ_H. Since the analog stage has a gain G_{IN}^{MAX}, 1 LSB of the ADC corresponds to a variation of ≈ 900 pA of the output current of the photodiode,

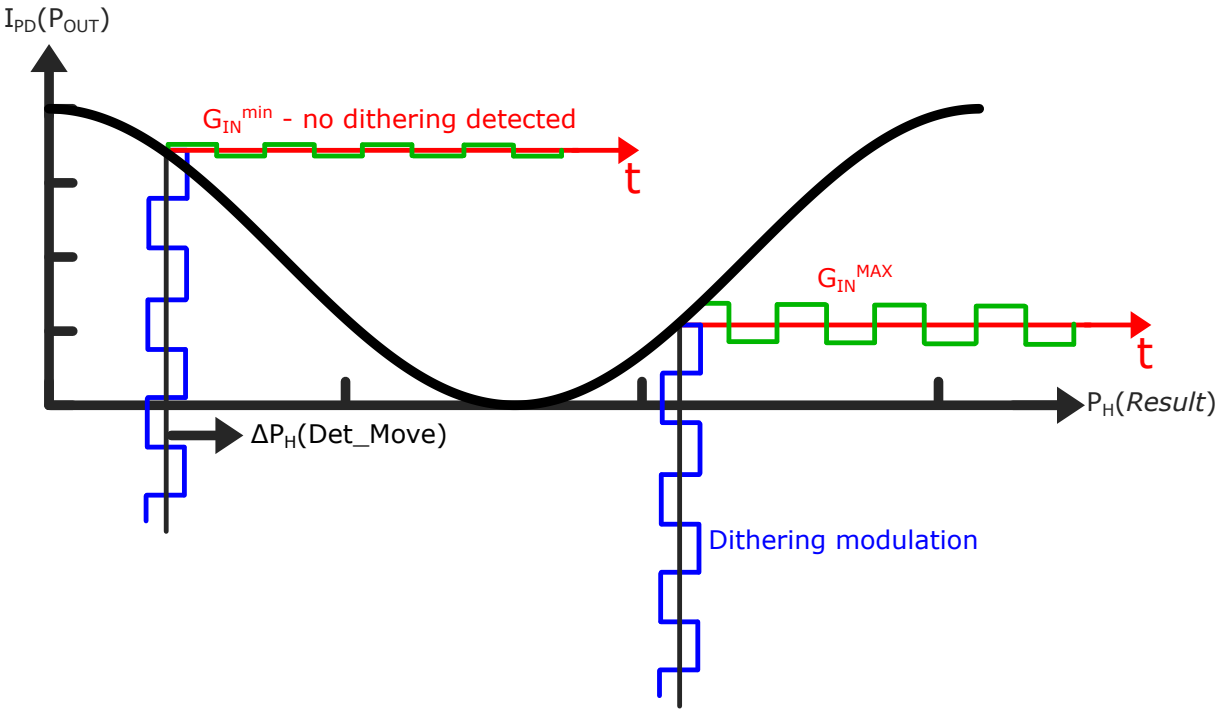


Figure 4.8: Different dithering amplitudes depending on the DC value of I_{PD}: the two points have the same slope, but different gain G_{IN} of the analog stage: one dithering signal will be detected, the other may not

equivalent to $\approx -60\,\text{dBm}$ of optical power variation: if noise (e.g. a thermal drift, way slower than the f_{dith}) modifies $I_{PD}(P_{OUT})$, dithering integration becomes effective and the system is driven towards the stable equilibrium point.

Troubles begin when the system inches closer to a maximum of $I_{PD}(P_{OUT})$: at some point, the dithering integration will become 0 and the integrator will start to modify *Result* by adding *Det_Move* until a new, non-nil dithering point is found. It is clear that this translates into a worse precision (with respect to the case of P_{OUT} minimization) in the control of the device, that eventually ends up locking right at the edge between the two regions (where the dithering technique is effective and where *Det_Move* has to be used), as shown in Fig. 4.9.

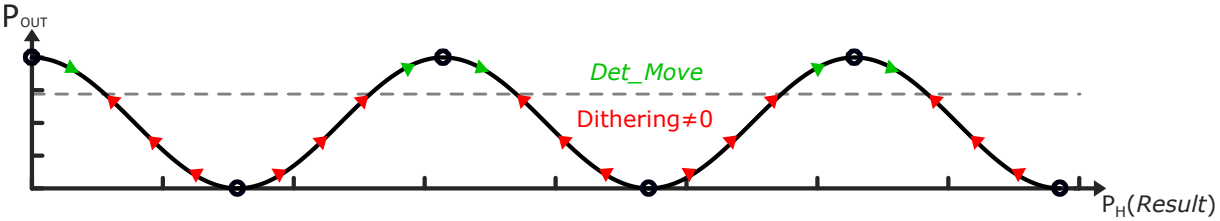


Figure 4.9: Schematic representation of the system trying to lock to a maximum of P_{OUT}

Finally, it is needless to specify that the the system either looks for a maximum or a minimum of P_{OUT} depending on the sign of the demodulation signal: if the samples related to a positive edge of the dithering modulation are subtracted and those related to a negative edge are added to *S_Result*, the control loop points towards a minimum, and viceversa. The choice is operated by the *Feedback_Sign* module, whose output is nothing but *De_Mod* XNOR *Sign*: depending on *Sign*, the demodulating signal is either in phase or in opposition with the modulating one and determines the sign of the feedback loop.

4.3.4. Reset of the integrator

The final functionality implemented in the integrator is a reset mechanism: in fact, it is possible that the MZI ends up operating in a region where dithering integration leads to the saturation of *Result* (either 6 V or 0 V on the heater) without finding, for example, any minima of the transfer function, as shown in Fig. 4.10.

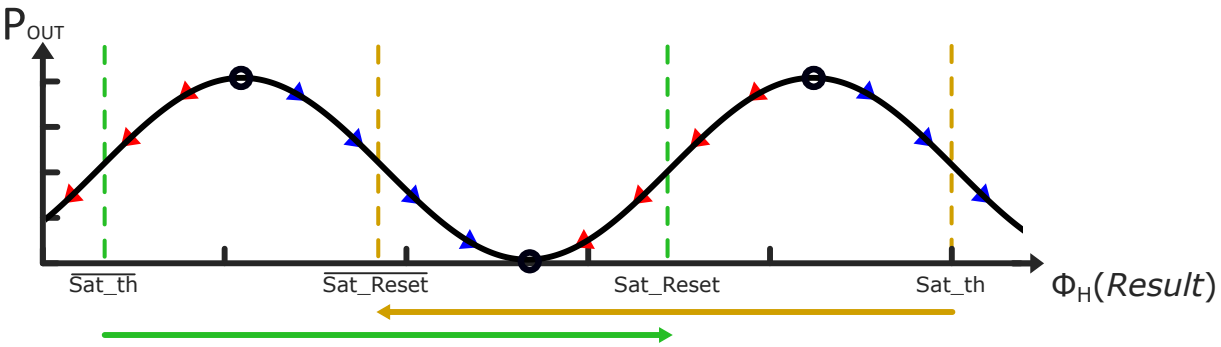


Figure 4.10: Principle of the reset mechanism: the working point is modified as much as needed to include a minimum and a maximum of $P_{OUT}(P_H)$

The problem is solved with the introduction of two parameters (*Sat_th* and *Sat_Reset*), defined by the user before activating the control loop. In particular:

- *Sat_th* sets both the upper and lower thresholds. To save area occupation, it is only 5 bits wide: the reset activates whenever, at the end of a full dithering period integration, the *S_Result*'s 5 MSBs match either *Sat_th* (upper saturation) or $\overline{Sat\_th}$ (lower saturation), meaning that the two threshold values will be symmetric with respect to the center of *S_Result*.
- When reset is activated, the value set on *Result* is either *Sat_Reset* (in case of lower saturation) or $\overline{Sat\_Reset}$ (in case of upper saturation), meaning that the integrator can be reset to two symmetric. This strategy allows, provided that the $\Delta\phi_H$ span covered by the heater is large enough, to always change *Result* so that the working

point of the MZI is shifted by at least a 2π, thus making sure that one minimum (or maximum, depending on what is being targeted) will always be present between the reset value and the threshold.

4.4. Modulation and demodulation timing

The whole dithering-based control strategy is effective only if a simple yet fundamental condition is met: that modulation and demodulation signals are properly timed. There are two requirements to be satisfied,both demanding particular care:

- The application of the dithering modulation on the heater should be synchronized with the conversion operated by the ADC and the analog reset of the gated integrator;
- The modulating signal should be properly delayed in order to generate a demodulation signal which is coherent with the sample to be added/subtracted in the integrator.

4.4.1. ADC synchronization

The synchronization that has to be implemented between dithering application to the heater and the gated integrator is shown in Fig. 4.11:

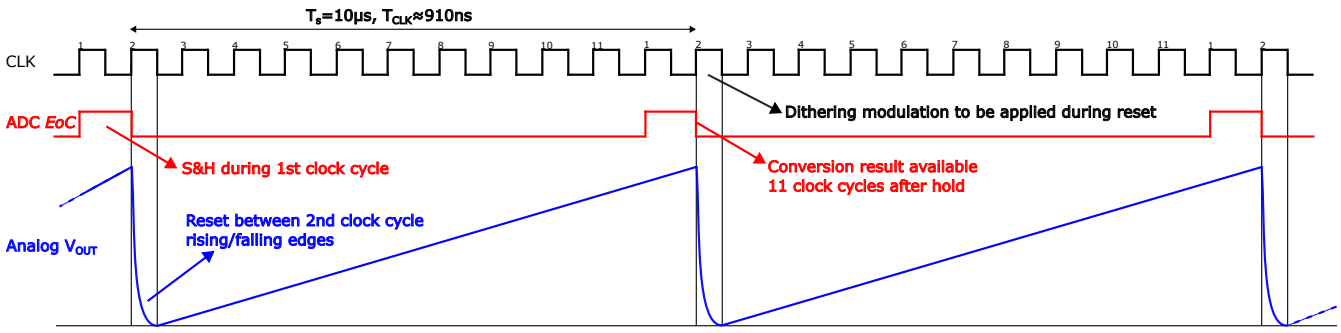


Figure 4.11: Waveforms of clock, ADC EoC and of the analog signal at the gated integrator output

At first, dithering application appears relatively easy: there are 2 synchronous modules, that are *Dith_Add* and *DAC_RW*, between the *Modulator* block that generates the dithering signal, introducing 1 clock cycle each of delay before the heater. The consequence is that when the ADC operates in continuous conversion the modulation signal should be generated on the rising edge of the 11^{th} clock cycle, so as to change the heater

voltage V_H on the 2^{nd} clock cycle.

This conclusion, which seems pretty straightforward, is not trivial when it comes to the very first conversion the ADC has to make after *Reset* has gone low, which ultimately determines the synchronization with the dithering signal: in fact, *Reset* is the signal available for the user to turn on/off the control loop, and it is asynchronous, meaning that a dedicated logic is needed to detect its transitions.

This is the task of the *Reset Delay* block. It samples *EoC* on the falling edge of the clock (in order not to risk to sample the signal twice, on 1^{st} and 2^{nd} clock rising edge) and then starts counting up to the 10^{th} falling edge: at the 11^{th} rising edge, the *Modulator* is finally "told" to start applying the dithering modulation to the working point. A consequence of adopting this strategy is that, after *Reset* becomes '0', before actually starting to sample a signal with modulation superimposed, the ADC delivers 2 further "meaningless" conversions: the one running at the moment of the *Reset* falling edge and the one produced by the sample taken on the first *EoC* after the event. They clearly impair the integration of the first dithering period, since *Gain Adjust* adds these 2 samples to the count up to 12 that determines *Dith_Over* to signal the end of a modulation cycle. This is, however, just a negligible drawback: *Reset* is supposed to make transitions either at the very beginning, when the ADC is first turned on, or run-time, when the user wants to open the control loop. In both cases, being *Reset* an external signal, the time scale involved in these operations is way longer than T_{dith}, making the loss of the first dithering integration after *Reset* goes low tolerable.

It is important to observe that also the *Start* signal of the ADC is asynchronous, as it comes from outside the chip; however, since both *Start* and *Reset* are external signals, their waveforms can be arbitrarily chosen: an intuitive way of using the two pins is to raise *Start* to '1' and to never lower it, keeping the ADC always on (declared typical power dissipation is 0.1 mW [24]), whereas *Reset* can be used to activate (when high) or to turn off (when low) the control loop.

A couple of final remarks should be made about the *Modulator* component:

- The dithering signal (*Dith_Mod*) is the result of the superposition of two square waves in phase quadrature: it has a periodicity of T_{dith}=120 μs, and it is sampled 12 times by the ADC ($T_S = 10\,\mu$s). During T_{dith}, it has to switch 4 times (with the sequence 00->01->11->10). Considering that 12 samples correspond to 132 clock cycles, the clock signal generating *Dith_Mod* should be 33 times slower than the master clock of the circuit: this is implemented through the *Clk_Div* module, whose output rising edges determine the states of the modulation signal (Fig. 4.12);

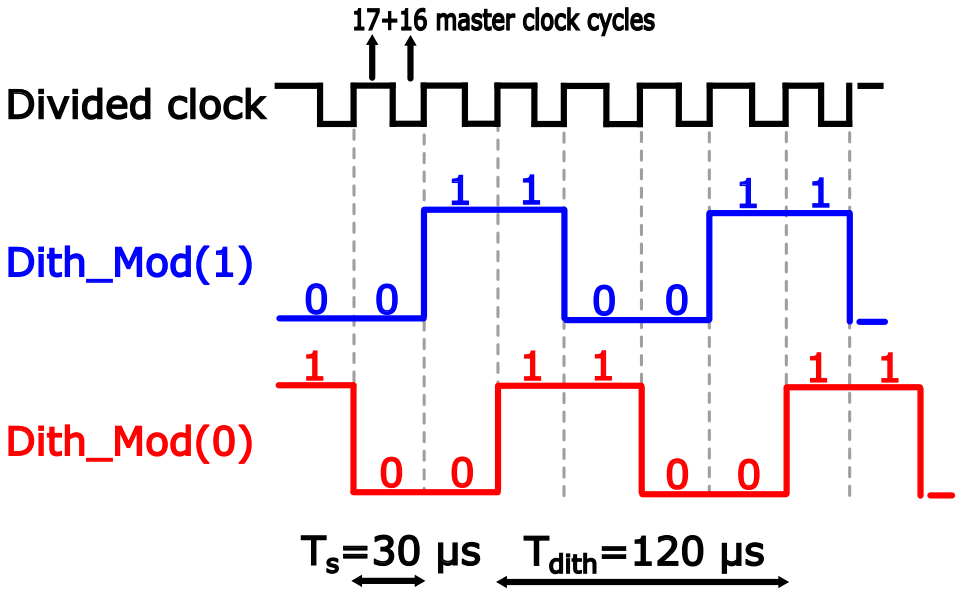


Figure 4.12: Waveforms of the signal that regulates the dithering modulation

- The only thing that really matters in this synchronization is that the dithering is applied on the heater on the 2^{nd} rising edge: the value of *Dith_Mod* on the first sample taken is irrelevant, as the system will always perform the integration of 12 samples, 6 carrying the positive edge and 6 carrying the negative edge of the dithering modulation.

4.4.2. Demodulation timing

In order to have a coherent demodulation of the dithering signal, *Dith_Mod* should be properly delayed before being fed to the integrator, and eventually inverted according to the sign to be given to the loop gain to steer the MZI either towards a minimum or a maximum.

This delay can be easily computed by looking to the chain that connects *Dith_Mod* to the integrator:

- As already stated, 2 clock cycles are needed for the dithering modulation to reach the heater, due to the presence of two synchronous modules in between (*Dith_Add* and *DAC_RW*);
- 11 clock cycles (10 μs) correspond to the duration of the analog integration of the photodiode current;
- An additional 11 clock cycles are needed for the ADC to convert the sampled analog value;

- 1 clock cycle is needed for *Gain Adjust* to evaluate the sample and feed it to the ADC, alongside the information about the the gain G_{IN} of the analog stage and the eventual notification that the dithering period is over;
- 2 clock cycles pass between the sample made available at the integrator input and the sampling of *Dih_Demod*, which is the delayed version of *Dith_Mod*, before finally making the addition/subtraction.

All these steps put together account for a total of 27 clock cycles (≈24.5 μs) between the application of the dithering to the current working point and the actual integration to determine the next one. It is thus safe to put a 22 clock cycles delay between modulation and demodulation: the value of *Dith_Mod* associated with the dithering sample i will be fed to the integrator after the $i\text{-}1^{th}$ has been summed and well before the next one becomes available.

The choice of the delay is not casual: 22 clock cycles correspond to the time needed by the ADC to complete 2 conversions. The consequence is that the ADC's *EoC* signal can be used as the clock for the delay cell *Demod_Delay*, allowing to save some silicon area (no need to count up to 22, two *flip-flops* are sufficient). It should be pointed out that this whole circuit, despite being implemented starting from a VHDL description, is **not** an FPGA, but an ASIC: there are no clock dedicated routes, meaning that whatever signal can be used to trigger *flip-flops*.

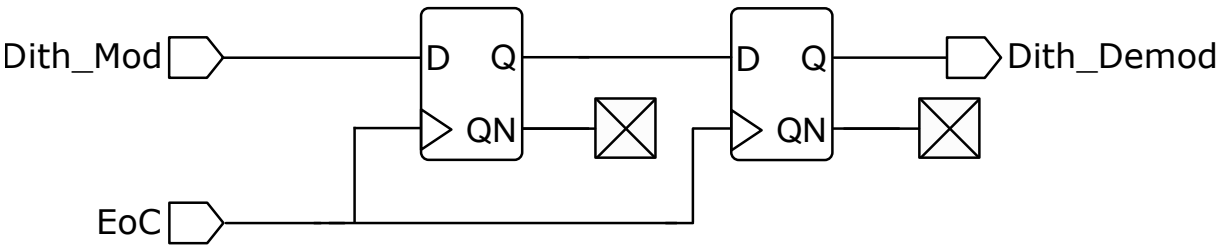


Figure 4.13: Simplified schematic for the delay of the modulation signal

4.5. Dithering addition, digital square root and external control of the actuators

To complete the digital chain, 3 final blocks are inserted between the integrator and the DAC that drives the heater, as reported in Fig. 4.14:

- The *Dith_Add* block is supposed to add (or subtract, depends on *Dith_Mod*) to *Result* the dithering zero-to-peak amplitude;

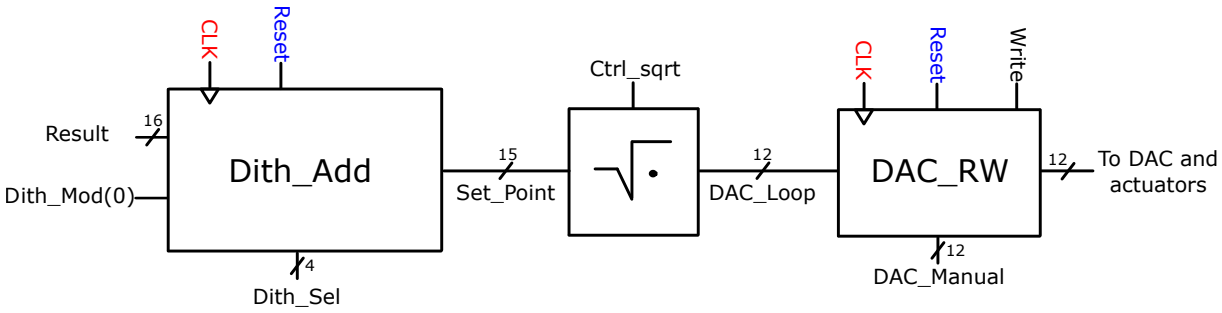


Figure 4.14: The final 3 modules of the digital chain complete of the respective pins

- *Square_Root* is a fully combinational block that eventually delivers a 12 bits wide digital word, proportional to $\sqrt{Result}$;
- Finally, *DAC_RW* is the module meant to feed the DAC with the information about the new working point, either set by the control loop or externally provided via the *DAC_Manual* pin.

4.5.1. Dithering Addition

The *Dith_Add* module was designed in order to grant the user the largest possible flexibility in choosing the amplitude of the dithering modulation. In particular, it is possible to arbitrarily select for each MZI of the mesh a different dithering amplitude: the 4 bits of *Dith_Sel* represent a thermometric code which determines 16 possible values for the *Dith_Amp* internal signal which is summed to *Result*. If $Dith\_Sel = N$, then *Dith_Amp* will have '1' in the N^{th} position, while all the other bits will be se to '0': as a result, the relation that holds true is:

$$Dith\_Amp|_{(Dith\_Sel=N)} = 2 \cdot Dith\_Amp|_{(Dith\_Sel=N-1)} \tag{4.2}$$

It is interesting to observe that the module only has a 15 bits wide output (*Set_Point*) despite the 16 bits of the input (*Result*): the reason is that, since *Dith_Amp* is the **zero-to-peak** dithering amplitude, in order to modulate only *Result*[0] (its LSB) it is necessary to add/subtract the 16 bits *Dith_Amp* corresponding to *Dith_Sel*="0000" (i.e. *Dith_Amp*[0]='1' and all the other bits set to '0').

Fig. 4.15 shows what is the main motivation behind this choice: the waveguides of each MZI of the mesh, as well as their output photodiodes, might receive a different amount of optical power depending on their position in the photonic circuit and, in general, to the total power circulating in the PIC. The consequence is that also the slope of $P_{OUT}(\phi_H)$ will

scale accordingly, meaning that for the same induced phase shift ϕ_H different dithering amplitudes will be detected. The possibility to tune the modulation for each device allows to compensate for this issue.

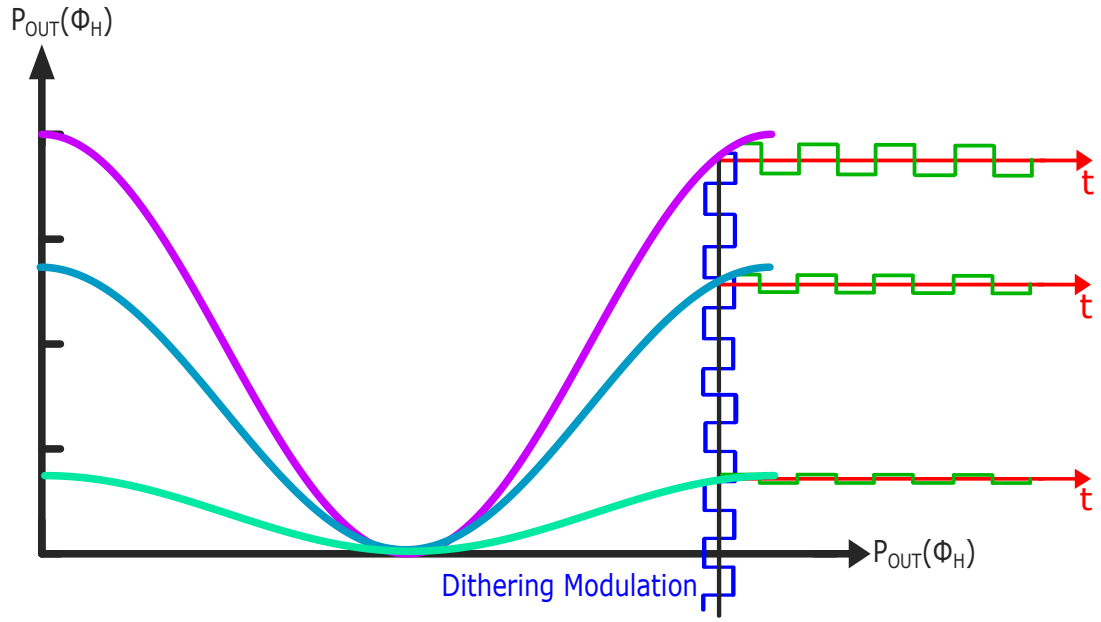


Figure 4.15: Different P_{OUT} modulation amplitudes for the same value of ϕ_H depending on the value of P_{OUT}^{MAX}

Finally it is worth observing that also a *Reset* pin is present: when *Reset*='1', i.e. when the user wants to stop the action of the control loop, no modulation signal is superimposed to the working point of the heater, which is left as it is and eventually modified via the DAC_RW moudle, described in the following.

4.5.2. Digital square root

The motivations behind the adoption of a module implementing a square root operation on the value to be passed to the actuators and its positive impact on the linearity of $P_{OUT}(V_H)$ has already been discussed in Chapter 2. As stated, the very simple yet effective solution that was implemented is the approximation of the square root with a series of lines with progressively scaling slope, as reported in Fig. 4.16.

The idea is to approximate with a different line each $[2^{2N}; 2^{2N+2}]$ interval of integers covered by the input word, with the respective linear function ranging between 2^N and 2^{N+1}. Choosing such intervals means that the first derivative's discontinuities of the approximated function will show up for the values of X that are digitally written with a '1' in an even position, and '0' for all the other bits. Maths can be done to prove that the

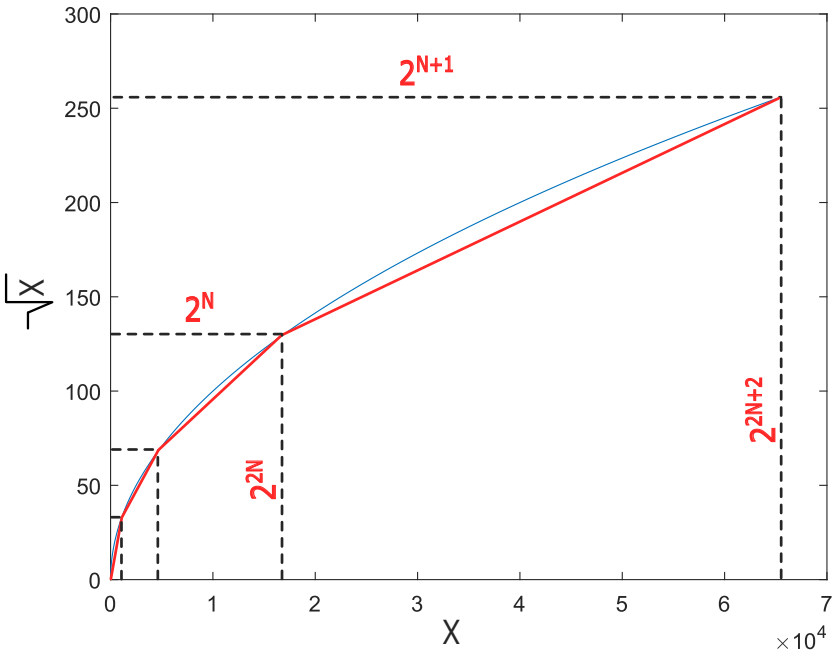


Figure 4.16: Visualization of how the function that approximates the square root is computed

equation describing each segment of the line can be written as:

$$\sqrt{X} \approx \frac{1}{3} \cdot (\frac{X}{2^N} + 2^{N+1}) \tag{4.3}$$

At first, the conclusion could be that the extraction of a $\sqrt{X}$ which has to be 12 bits wide requires a 24 bits input. It must be observed, however, that to implement a division by an odd number, as requested in Eq. 4.3, is quite a bulky operation to be performed at digital level, whereas the other two operations (the division by 2^N and the addition of 2^{N+1}) are very simple. It is thus convenient to accept the introduction of a factor 3 in the loop gain and to deliver, as the output of the module:

$$3 \cdot \sqrt{X} \approx \frac{X}{2^N} + 2^{N+1} \tag{4.4}$$

This has a consequence on the number of bits required at the input of the module: since, from Eq. 4.4, the 12 bits wide output now is $3 \cdot \sqrt{X}$, the range of X values that produce a valid output should be divided by a factor 9, thus reducing the required number of input bits from 24 to 21 (necessary to represent $\frac{2^{24}}{9}$).

There is only one last question to answer: if Eq. 4.4 proves that the input of the

Square_Root module has to be 21 bits wide, how come the actual input signal *Set_Point* only has 15 bits? The reason is that, in order to simplify the circuit and reduce its area occupation, 6 LSBs have been excluded from the algorithm: no square root operation is done in the range [0;2^6-1] of input values (considering a 21 bits wide input X). This is not a problem at all: with respect to a 21 bits wide word, the 6 LSBs are so irrelevant that it is reasonable to assume the value 2^6-1 to fall inside the region where the reset mechanism of the integrator will be triggered.

Finally, it should be mentioned that it is always possible to turn-off the square root operation with the *Ctrl_sqrt* pin: if it is set to '0', the output *DAC_Loop* will just be equal to the 12 MSBs of *Result*, as schematically shown in Fig. 4.7.

4.5.3. Externally driving the actuators

As stated, it is always possible, through the *Reset* pin, to completely suspend the control loop and to fix the working point of the heater to the present state.

In addition to that, the *DAC_RW* module allows to externally set the digital word to be fed to each DAC at a desired level, stated by *DAC_Manual*. The whole operation unfolds in this order:

- The *Reset* pin is raised to '1', so as to stop the control loop;
- *DAC_Manual* is fed to the DAC only when also *Write* is raised to '1', otherwise the output of *DAC_RW* remains equal to *DAC_Loop*, i.e. the last working point determined by the integral control loop;
- *DAC_Manual* is fed to the DAC **only** if both *Reset* and *Write* are set to '1'. It is not possible to set a user-defined working point when the control loop is active.

4.6. Shift Registers

There is one final part of the digital circuit that has to be described. Many of the modules require some fixed parameters, defined at the beginning of the operation and tunable depending on the application; at the same time, it would be too risky to rely only on the output of the photonic integrated circuit for proper monitoring and eventually debugging the proposed architecture, and the possibility of internally sampling the state variables of each channel would be a useful feature. These two read/write functionalities are implemented by mean of two shift registers.

4.6.1. Write shift register

A SIPO (*Serial Input Parallel Output*) has been described to deliver all the modules with the proper digital words. The choice of a serial input is dictated by the criterion of using the smallest possible number of pads to connect the electronic chip to the external world (each pad in AMS C35B4 occupies between 5'000 and 10'000 μm^2). Considering a mesh of 7 MZIs, a total of 7 channels will have to be integrated for a full control of the photonic circuit (in general, a diagonal mesh with N inputs require N-1 control channels). It is thus possible to evaluate the size of the shift register since:

- *Gain_Adjust* requires 10 bits to set the two threshold needed for the evaluation of the ADC sample;
- Four parameters have to be defined for the *Integrator*: *BW_Gain* (4 bits), *Det_Move* (16 bits), *Sat_th* (5 bits) and *Sat_Reset* (16 bits), for a total of 41 *flip-flops* needed by the module;
- *Dith_Sel*'s 4 bits have to be defined to set the desired amplitude of the dithering modulation. As stated in Sec. 4.5.1, a different amplitude of the dithering signal can be chosen for each interferometer: in a 7 MZIs system a total of 28 bits will be needed;
- 2 bits are needed by *Ctrl_sqrt* and *Feedback_Sign* to determine, respectively, the choices about making or not the square root before feeding the DAC and about locking the system to the minima or the maxima of the MZIs' $P_{OUT}(\phi_H)$ transfer functions;
- Each channel has 2 DACs, and for both of them it is possible to externally state the digital word to be applied to the heater. As a consequence, 12 bits are needed to specify the respective *DAC_Manual* word, and an additional one that carries the information of the *Write* command. In a 7 MZIs mesh (14 DACs), a total of 182 bits will thus be needed.

It should be pointed out that, apart from *Dith_Sel*, *DAC_Manual* and *Write*, all the other parameters are shared between all the channels of the system, allowing to save some space. The tally reveals that a 263 bits SIPO shift register has to be implemented, like the one reported in Fig. 4.17.

In addition to the input *Bit_In* that serially feeds the register, there is also a control pin *New_In* that signals whenever a new bit is available at input side and indicating that the register can make a shift. It is important to observe that the *New_In* cannot be

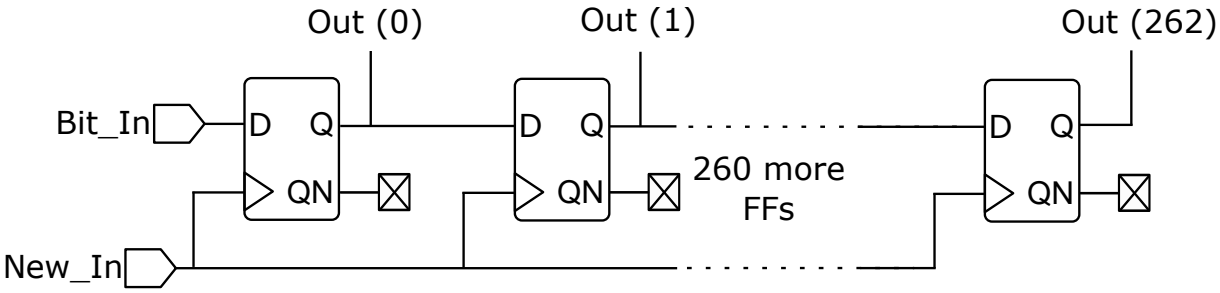


Figure 4.17: Scheme of the input shift register

connected to the master clock of the integrated circuit: the serial data that enters the register comes from the external world, i.e. it is an asynchronous signal that may change with a frequency slower than $f_{CLK} = 1.1\,\text{MHz}$. As a result, two pads will be needed to connect the input ports of the shift register.

4.6.2. Read shift register

Differently from the *Write* shift register, a PISO (*Parallel In Serial Out*) *Read* shift register is not mandatory, but it might be very useful in order to monitor the system and eventually correct any error in the settings of the input parameters according to the application requirements.

In particular, it is interesting to extract the information about the light intensity impinging on the photodiode and the control voltages applied on the heaters. To achieve this scope, the register should be sized to allocate for:

- 10 bits of *ADC_sample* to tell the latest value sampled by the converter;
- 3 bits of *TIA_gain* that, combined with those referring to the ADC sample, allow to evaluate the light intensity impinging on the photodiode;
- 24 bits (two 12 bits long words) representing the digital words converted into the voltages $V_{H1,2}$ of the actuators.

All these parameters are obviously peculiar to each channel of the chip: as a result, in case of a 7 MZIs mesh, the *Read* shift register should allocate for a 259 bits wide digital word.

The operation of the *Read* register is slightly more complicated than the *Write*'s. In fact, the 4 values reported in the register dynamically change during the operation with a frequency as fast as f_S =100 kHz, i.e. every 10 clock cycles, for what concerns (*ADC_Sample* and *TIA_gain*), whereas the DACs' output are simultaneously updated

every $T_{dith} = 120\,\mu$s. The external read-out system to which the register is connected through the *Out_Bit* pin might not be fast enough to read 259 bits within $T_S = 10\,\mu$s. The solution proposed is to accept that the information contained in the register, which is constantly updated through its parallel input pins, can only be read every once in a while: as long as the *Get_Bit* (coming from a dedicated input pad) is low, the register is constantly being updated with the information provided by the loop; as it goes low, the word stored in the register is freezed and read, one bit at a time, whenever a rising edge of *Read_Bit* is detected. This register thus require 3 pads to work properly: *Get_Bit* to start/stop its updating process, *Read_Bit* to allow data to be fed to the external world, whose port is *Out_Bit*.

4.7. Area estimation

One brief comment has to be made about the area occupied by the digital circuit. It should be taken into account that, in a N channels control system, there are some modules have to replicated only once (such as the shift registers) and others that need to be replicated in every channel of the system, even more than once. Tab. 4.1 summarizes the area occupation and the cardinality of each block[3].

Module Name	**Single module area** $[\mu m^2]$	**N. of modules**
ADC	82'500	N
Gain_Adjust	10'600	N
Integrator	73'000	2·N
Dith_Add	12'600	2·N
Square_Root	5'500	2·N
DAC_RW	4'100	2·N
Modulation and Timing	9300	N
Write_Register	67'800	1
Read_Register	86'400	1

Table 4.1: Estimated silicon area occupation of the digital circuit

Where the area occupied by the shift registers has been considered for a 7 MZIs system (i.e. N=7). It is possible to conclude that each channel of the system is integrated, for what concerns its digital part, over an area of $\approx 315'000\,\mu m^2$. This is a dominant value

[3]Area estimation is done with a dedicated function of Cadénce *Genus* [25].

with respect to the analog part and demonstrates one more time the enormous advantages that the adoption of a technology with smaller feature size would bring to the chip.

5 | Conclusions and future developments

"Questa conclusione, benchè trovata da povera gente, c'è parsa così giusta, che abbiam pensato di metterla qui, come il sugo di tutta la storia. La quale, se non v'è dispiaciuta affatto, vogliatene bene a chi l'ha scritta, e anche un pochino a chi l'ha raccomodata. Ma se in vece fossimo riusciti ad annoiarvi, credete che non s'è fatto apposta" [28].

This thesis went into the details of a possible architecture for a control system meant to stabilize and reconfigure a *mesh* of Mach-Zehnder Interferometers built with Silicon Photonics technology. In consideration of the integrated nature of the optical circuit, the choice for the dedicated electronics fell on the ASIC approach, to take full advantage in terms of compactness, speed and limited power dissipation allowed by the CMOS process.

For what concerns numerical results, the integral control strategy proposed, based on the dithering technique, allowed to steer each interferometer either towards a minimum or a maximum of the transfer function thanks to the possibility to extract the information about the sign of the first derivative. In particular, loop gain was computed for the particular case of the device locked to a minimum, demonstrating an achievable bandwidth up to the $\approx$ kHz range, almost a factor 10 better than previous designs [12].

The analog front-end was designed in order to be able to manage a wide range of input currents, from 850 μA down to 150 nA. To face the limited resolution of the ADC (only 10 bits in spite of a required rejection ratio of 40 dB), an automatic analog gain adjusting network was designed, allowing to map with a more than acceptable resolution the most critical region of the MZI's transfer function, i.e. the one around its minimum. Noise of the input stage was limited well below the quantization error of the ADC. In addition to that, when the system locks to a minimum of the transfer function the dominant noise contribution is the shot noise associated to the optical signal impinging on the photodiode, while electronics' contribution is negligible.

Most of the improvements with respect to the previous, fully-analog architectures were made possible by the introduction of a digital circuit, that boosted both performances

and functionalities of the system. in particular:

- The bandwidth of the system was made adjustable at digital level: the user can set a different weight of the samples to be integrated, allowing the bandwidth to span from kHz down to a fraction of Hz;
- The detrimental non-linearity descending from the quadratic relation between heater voltage and induced phase shift was compensated with the introduction of a block that implements an approximation of the square-root operation at digital level;
- Two shift registers were introduced to allow the setting of almost all the parameters of the circuit, the possibility of monitoring and storing information about the working point of the devices (heaters and photodiode) and to eventually deactivate the control loop in order to externally force the voltage to be applied on the thermal actuators;
- The occupied area proved that this ASIC could be easily used to control at least an 8-inputs MZIs diagonal mesh, although thanks to the modularity of the architecture the whole circuit could be easily replicated in order to control circuit with at least a doubled complexity.

5.1. Future developments

There is still some work to be done before the actual deployment of this promising chip to real-life application. This includes:

- The layout of the electronic ASIC will have to be submitted to the foundry (via the *EuroPractice Service*) for the integration of the circuit on a silicon wafer;
- Testing will have to be done for the characterization of the device, alongside the development of the electronics necessary for the control and the connection of the circuit to the external world (e.g. power supplies, input and output data buses...);
- Finally, the system will be connected to a mesh of Mach-Zehnder Interferometers for its actual application in a photonic circuit;

In parallel to these tasks, the transition to a smaller technological node should be taken into account to fully exploit all the advantages coming together with the intrinsic scalable nature of digital circuits.

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Ringraziamenti

Se non potete parlare bene di una persona, allora non parlatene.

Di solito, o perlomeno questo è quello che ho avuto modo di osservare in quasi tutti i miei predecessori, i ringraziamenti sono quella parte che si scrive alla fine della tesi, a detta di molti quando si è da un pezzo oltrepassato il limite dell'esaurimento nervoso per il troppo lavoro, e con l'acqua alla gola perché ormai non resta più molto tempo per dare alle stampe questo calepino di dubbia utilità, questa *petite affaire toute serieuse*. Ecco, col dovuto rispetto per quei *giganti sulle cui spalle come nani siamo sollevati* e che si sono laureati prima di me, credo che questa sia una ingenuità: mentre il corpus della tesi suscita l'interesse del solo autore, talvolta di relatore e controrelatore e, per i più fortunati, di quelli che *sono subentrati nella vostra fatica*, l'elzeviro finale desterà l'interesse di tutti *i miei venticinque lettori*, dunque perché scarabocchiarlo in fretta e furia a ridosso della laurea? Ecco perché ho deciso, con tutta calma, di scriverlo ora, come mia prima fatica letteraria, e avere così due mesi di tempo per aggiustarlo e raffinarlo. Prima di iniziare, voglio proporvi un piccolo gioco, che renda un po' interattiva questa lettura: qua e là, evidenziate in corsivo, sono disseminate citazioni e semicitazioni tratte da libri, film, canzoni, personaggi storici e, perché no, anche da qualche memotto. Insomma, *un regalo di un piccolo e distante pianeta, un frammento dei nostri suoni, della nostra scienza, delle nostre immagini, della nostra musica, dei nostri pensieri e sentimenti*. Vogliate divertirvi, se vi va, a verificare quante di queste frasette vi siano già note, consapevoli che questo non vuole assolutamente essere un presuntuoso esame di cultura generale: è semmai uno strumento per verificare quanto simili siano i vostri interessi a quelli del modesto scribacchino che con questa introduzione vi ha già sottratto abbastanza tempo. Buon divertimento!

Ora non voglio assolutamente fare il moralista, che *a forza di discutere di etica non ha poi il tempo di praticarla*, però una considerazione la voglio fare, voglio predicare una convinzione da tempo radicata in me e che questo anno di LabSAMP ha fatto germogliare e fiorire. È la certezza che da soli non si va mai da nessuna parte, e che i successi personali, semplicemente... non esistono. Quel poco che ho realizzato, in qualsiasi ambito e a maggior ragione durante questo percorso di tesi, l'ho realizzato solamente grazie alla *social*

catena formata da un numero impressionante di uomini e donne con cui ho condiviso pezzi di percorsi, alcuni lunghi qualche giorno, altri tutta una vita: sulla laurea ci sarà solo il mio nome, ma chi sarebbe tanto sciocco da pensare che quel nome (che, tanto per cominciare, non ho scelto io) stia scritto lì unicamente per merito mio? Volente o nolente, in ogni sfida sono sempre parte di una squadra, e sarò perennemente insoddisfatto se cercherò il successo unicamente per me: *o noi risorgiamo adesso come collettivo, o saremo annientati individualmente*. Ecco perché, ora, intendo passare in rassegna tutte le squadre insieme a cui posso dire di aver *combattuto la buona battaglia, terminato la corsa, conservato la fede*.

Sicuramente la squadra in cui conto più presenze è la mia famiglia, il cui cognome *with pride I wear it to the grave*: è l'unica che non mi sono scelto, ma anche, ne sono sicuro, la migliore che mi potesse capitare. A cominciare dalle mie nonne e da quei nonni che non ho mai conosciuto: penso soprattutto a voi quando dico che sarebbe da sciocchi prendere per sé tutto il merito di questa laurea. Se oggi sono qui, è anzitutto per la vita di rinunce e sacrifici che voi avete fatto al posto mio. Sentirò sempre addosso la responsabilità di dover cogliere tutte le opportunità che voi non avete avuto. Opportunità, lasciatemelo dire, che vengono dall'unico cosiddetto "ascensore sociale" di *questo benedetto, assurdo Belpaese*: la tanto bistrattata scuola, pubblica e gratuita.
Papà: mi conosci e sai che l'autostima non mi manca, ma in tutti questi anni mi ha dato una forza incredibile sapere che, comunque fossero andate le cose, avrei sempre avuto una persona che avrebbe sempre tifato incondizionatamente per me.
Mamma: spesso e volentieri ti prendi qualche parere (il più delle volte, va detto, meritato), ma sappi che da te ho imparate più cose che da qualsiasi altro insegnante.
Elena: non andrò a mentire, se tu non ci fossi stata sarei stato molto meno, quasi per nulla, motivato in tutti il mio percorso scolastico e, già lo so, anche in quello lavorativo. Ai miei occhi sarai sempre quella intelligente della famiglia, l'unico traguardo che ha senso vantarsi di aver raggiunto, le poche volte che ci riesco. Se penso a una persona cui dedicare l'incipit di questi ringraziamenti, sei sicuramente tu.

Paese mio che stai sulla collina, luogo *ove il tempo mio primo si spendea e la miglior parte*! Non posso che pensare con gratitudine a questa comunità educante di persone per molti versi straordinarie, per altri solo bizzarre, in ogni caso uniche, che mi ha accompagnato in questi 25 anni. A tutti i miei amici galbiatesi va un grazie per la comprensione mostrata: non avete mai rinunciato a me, nonostante tutte le volte in cui, pur di raggiungere questo traguardo, io ho dovuto rinunciare a voi. E guardando giù per la 500esima volta e forse più dalla vetta del monte Barro, quella che mi è più cara fra le *cime inuguali, note a chi è cresciuto tra voi, e impresse nella sua mente, non meno che lo sia l'aspetto*

de' suoi più familiari del nostro territorio, mi convinco che anche se il mio futuro, con molta probabilità, sarà lontano da Galbiate, io resterò per sempre un Galbiatese. *Ti do l'appuntamento come e quando non lo so, ma so soltanto che ritornerò!*

Un pensiero lo voglio poi rivolgere a quella palestra di vita che è l'arbitraggio e a quella seconda famiglia che è la Sezione AIA di Lecco. Due cose mi ha dato, e mi sta dando, questa esperienza: una valanga di vestiti e un sacco di amici. Originali entrambi. E qui voglio riportare la frase di un mio Organo Tecnico, tale Giuseppe Provesi, che soleva (suole, è ancora vivo) ripetere: "quando pensi di non essere all'altezza della partita da arbitrare, ricorda che chi ti designa di calcio ne sa più di te, e sa che sei in grado di vincere la sfida". Ecco, nella sua semplicità questo ragionamento mi ha sempre dato forza nei momenti di sconforto e paura, ovviamente anche al di fuori del mondo del calcio.

Infine, grazie agli amici con cui ho condiviso centinaia, se non migliaia, di chilometri di corsa. Ne voglio nominare solo tre, perché onestamente servirebbe un'altra tesi solo per includere tutti gli Sky Lario Runners: *il Giovane Favoloso* Ferruccio Colombo, *la Locomotiva Umana* Gaetano Appiani e *l'Eroe dei Due Mondi* Paolo Confalonieri. Premetto che, proprio come al rumore 1/f, ci ho sempre creduto molto poco a quella narrativa del "andare a correre libera la mente", "ti fa sentire in sintonia con il mondo", "le migliori idee vengono quando sei in giro di corsa"... mi sembra della grande aria fritta, giustificazioni inutili, *non riuscivano a credere che uno poteva correre tanto senza una ragione particolare*. L'unico vero effetto collaterale che riconosco a questo sport è avermi fatto incontrare persone a cui guardo e di cui penso: "voglio diventare come loro" (oltre a darmi, *questo lo dobbiamo dire con grande chiarezza*, la possibilità di mangiare di tutto senza ingrassare, che sempre sarà lo scopo primo della mia corsa).

Un momento, qualcuno ha detto "infine"? Non manca qualcosa, o qualcuno? Mio fratello in Cristo, non siamo nemmeno a metà dei ringraziamenti! Perché ora viene la squadra per cui ho giocato in quest'ultimo anno, e di cui sogno di diventare una bandiera, di cui *per sempre vivrò, con questi colori nella testa*: quel LabSAMP al quale manca solo un posto letto per convincermi ad abitare lì. Ma andiamo con ordine, immaginandomi di entrare in Lab, come ogni giorno, alle 8 del mattino, di salutare il prof. Ferrari e Vittoria e quindi, presa posizione alla mia postazione, di impallinare tutti coloro che entrano col consueto "ciao [nome], ben arrivata/o!". Con questo giochino mentale dovrei riuscire a non dimenticare nessuno.
Il primo "grazie" e uno dei più sentiti va sicuramente a quel *ragazzo un po' stagionato ma con il cuore sempre giovane* che è il prof. Marco Sampietro: aver accettato la sua proposta di tesi è, al momento, il "sì" più azzeccato della mia vita. Se questo posto è, con ogni probabilità, il miglior ambiente di lavoro di tutto il Politecnico, il merito va

anzitutto a chi lo dirige, la cui forma mentis viene a cascata fatta propria da tutti gli altri collaboratori (e anche il modo di parlare, soprattutto per chi come me ha la scrivania praticamente di fronte alla sua, senza ostacoli di mezzo).
Ora, sono convinto che il talento, proprio come *il coraggio, uno, se non ce l'ha, mica se lo può dare*; si può però compensare con l'impegno, e pervenire ai risultati col duro lavoro e la giusta mentalità. Il prof. Giorgio Ferrari, per me, è la sintesi di tutto questo: un uomo che a delle capacità fuori dal comune unisce una dedizione e una cultura del lavoro che non ho mai incontrato in nessun altro, e ogni giorno, col suo esempio, mi ricorda che *a chi fu affidato molto, sarà richiesto molto di più*. Non ricordo una singola riunione con lui da cui non sia uscito dicendomi: "sì, ce la posso fare", il più delle volte dopo essermi presentato con *cinque pani e due pesci* di idee. E no, il miracolo non l'ho mai fatto io.
Passando allo sgabuzzino dove "sì ecco, insomma, qua è dove lavorano, o comunque dovrebbero lavorare i nostri integrati...", il primo pensiero corre al Dottor Toso: *"Tu se' lo mio maestro e 'l mio autore, / tu se' solo colui da cu' io tolsi / lo bello stilo che m'ha fatto onore"*. Non lo nascondo, sento addosso il peso della responsabilità di dover prendere il tuo posto, soprattutto a tavola. Mi sento poco più che un *costruttore di soffitte*, e l'idea che fra 3 anni, forse, tu e io avremo in tasca gli stessi titoli rende l'idea di quanto mendaci siano gli stessi.
Gabu, non ironicamente penso che in pochi lì dentro mi conoscano bene quanto te, nessuno come te può capire quanta frustrazione ci sia dentro chi sbraita *"dai, Cadénce, come fai a darmi warning? Ma come fai a darmi warning? Madonna, oh!"*, quanta pazienza, intesa nel senso letterale di "capacità di soffrire", serva per lavorare su quelle scrivanie. Sono sicuro che avrai successo in qualsiasi squadra andrai a giocare, perché, lasciatelo dire, ho conosciuto pochissime persone con la tua stessa elasticità mentale e rapidità di apprendimento, e ancora meno col tuo stesso talento nel riuscire a sembrare serie anche quando sono piene di alcol.
Alex, sono abbastanza convinto che più di una volta tu sia andato a casa pensando: "ma questo è fulminato". Può pure darsi che abbia ragione, ma sono ancora più convinto che insieme possiamo fare grandi cose: che effettivamente le faremo poi è un altro paio di maniche, del resto *essendo noi uomini medi, le vie di mezzo sono, per noi, le più congeniali*.
Sebastiano, la reazione ammirata e stupita delle persone quando gli dico che lavoro a fianco di un fisico teorico dimostra una volta di più che l'abito fa il monaco, eccome. In realtà so che "lavoro" vicino a un amico, una persona dalla cultura smisurata, un uomo veramente di Sinistra (e sai quanto per me questo valga come un complimento). E, lasciatemelo dire senza *criminoso ottimismo*, sei il miglior spot della capacità del LabSAMP di integrare nuovi elementi.

Cristina, Elisabetta, *anche così è stato breve il nostro lungo viaggio*, ma vi penso spesso e con gratitudine per avermi fatto sentire uno di voi anche in quei primi tempi (molto brevi) in cui, giustamente, lì dentro non ero nessuno; e il vostro ricordo vivrà con Vittoria, *et a nullo tenebris damnabimur aevo.*

Giovanni, sappi che i ringraziamenti scritti in fondo alla tua tesi sono il motivo per cui ho deciso di dedicarmi ai miei con tanto anticipo. A suo modo è anche questo un insegnamento, di cui ti ringrazio.

Giulio, l'amico Giulio! Che amicizia meravigliosa mi son perso in questi primi cinque anni, che onore enorme sarebbe poterla proseguire nei tre e spero i molti più che verranno! Le nostre origini e la nostra formazione, decisamente simili - perché Galbiate è molto più vicina a Specchia che a Milano - ti hanno permesso di conoscermi meglio di chiunque altro lì dentro, *mi scruti e mi conosci* al punto che *la mia parola non è ancora sulla lingua e tu già la conosci tutta.* Il valore delle persone a cui potremmo subentrare ci carica di una responsabilità enorme, ma doverla sostenere insieme a te mi rincuora, perché so che ora *il mio giogo è dolce, e il mio peso leggero.*

Diego, non mi stancherò mai di ripeterlo, come tu non ti stancherai mai di fare finta di non crederci: per me sei il vincente per definizione, la personificazione del mantra per cui *tra giocar bene e vincere ci passa una roba sottile che sembra sottile... ma non è sottile.* Spesso e volentieri mi capita di guardare la tua sedia, e il monito scritto alle sue spalle, e pensare che Diego Barbieri *era il migliore che avevamo in questa fogna. Diego Barbieri era il primo e unico tesista che abbia mai incontrato che si preoccupasse come me. E non è importante il fatto che lui fosse uno studente eccezionale. La cosa importante è che era... che è una persona eccezionale. Per questo la gente lo adora. E anche io. Era mio amico.*

Un pensiero a quel guerrafondaio di Gabriele: se è vero che *solo i cinici e i codardi non si svegliano all'aurora*, all'ora dell'alba lui tipicamente è ancora sveglio dal giorno prima, con un ritmo circadiano perfettamente complementare al mio. Questo non ci ha impedito di vivere momenti a dir poco epici insieme: stiamo tutti pensando a quella volta che facemmo esplodere, pugnalandolo con un cacciavite, un barattolo di lenticchie sulla scrivania di un ignaro Alex (che giustamente il giorno dopo si insospettì, trovandola così pulita). Perché vedete, non è la quantità che conta: *per me è la qualità, la freschezza!*

Beppe, più di chiunque altro conosci la fatica che si fa a scrivere racconti di proprio pugno, che siano questi ringraziamenti, pagine di diario che riassumano una serata o pagelle ignoranti che la valutino. Ma come tirarsi indietro da queste dolci fatiche? Del resto *si fa bene a tenere un diario, ed è utile che molta gente lo sappia.* L'idea che tu, trapiantato a Milano da anni, sia solo una versione mitigata di *chi vive in Calabria*, mi spaventa e a un tempo mi affascina: che sogno sarebbe tornare a Cirò in tua compagnia! Non ti ho mai

sentito dire nulla di banale, nulla di prevedibile: poeta, attore, pittore... tu sei uno dei miei artisti preferiti, e uno dei più completi che conosca.
Vittorio, *io non ci credo al caso, io credo alla volontà di Dio*, e per questo son convinto che ci deve essere un disegno dietro la tua collocazione così azzeccata all'interno del laboratorio, esattamente al centro, cosicché tutti possano ricevere in egual misura l'entusiasmo che sai irradiare. *Quando partisti, come son rimasta! Come l'aratro in mezzo alla maggese*: abbiamo provato a rimpiazzarti con la piantina che porta il tuo nome, ricevendo in cambio, però, solo ossigeno e nulla di più. L'idea che fra un mese dovremo fare a meno della tua luce un po' mi spaventa, posso solo prometterti che farò tutto il possibile per essere degno erede di tanto clown, perché *ogni caduto somiglia a chi resta, e gliene chiede ragione*.
My name is Federico Monti, but everybody calls me... Frode. E se ne va, saluta il LabSAMP a bordo della sua bici elettrica, o meglio: elettrificata. Questo ammiro di te: la tua capacità e la tua forza di volontà, mancanti nella maggior parte dei tuoi colleghi, me compreso, di tradurre in pratica le tue conoscenze di elettronica, di applicarle artigianalmente alla tua vita quotidiana. Vivido resterà il ricordo di quella passeggiata esaltata, come un pugile sul ring che ha appena mandato al tappeto l'avversario, il giorno che scopristi che la tua amata bicicletta esisteva ancora, e che avevi la possibilità di recuperarla. Adoro le persone che non nascondono le proprie emozioni. Ora ti abbraccerei, se solo avessi braccia abbastanza lunghe per cingere tanta grossezza, che aumenta giorno dopo giorno.
Riccardo, del cui titolo di Re degli Uomini mi faccio vanto di averti investito. *I campioni sono così*: in quello che fanno ci mettono solo e tutto il cuore. Da te, più che da chiunque altro, ho imparato cosa voglia dire fare, anzi, essere parte di questa squadra: e cioè che i ragazzi vanno sostenuti sempre, soprattutto nelle difficoltà. Ora che anche Diego, il nostro campione, se ne è andato, la tua leggendaria tazzina del caffè è capitata in eredità a me: ti prometto che la custodirò *come pupilla degli occhi*, e la riserverò come massimo onore per gli ospiti più illustri del LabSAMP.
Cainã, come dimenticare quel pomeriggio in cui, da vero gigachad con la borsa tematica, mi appoggiasti una mano sulla spalla e, col tuo accento così dolce, commentasti: "oh, complimenti per il dottorato!". Devo ammettere che, a parte l'immediata reazione da *ma che cazzo stai dicendo, mi prendi anche per il culo?*, è stato uno dei momenti più divertenti vissuti quest'anno. Mi auguro di tutto cuore che nei prossimi tre ne vivremo molti altri, tanto in laboratorio quanto, perché no, su un campo di calcio, da compagni in quella squadra, quella dei dottorandi, in cui sogno di giocare sin da bambino.
Paola, non nascondo che ho sempre avuto un debbole per questa "brillante neolaureata magistrale de Roma nord", per il suo buffo modo di parlare che non mi annoierebbe nemmeno se declamasse l'elenco telefonico, per lo *slancio generoso, fosse anche un sogno matto* con cui trascina il LabSAMP in avventure difficili da dimenticare. I più corag-

giosi, o semplicemente il più incosciente (il singolare non è casuale), li trascina anche nella preparazione di manicaretti che ogni volta alzano l'asticella di ciò che si può cucinare con un bollitore e un forno a microonde, e puntualmente vanno a occupare una posizione sul podio dei pranzi più gustosi che io abbia mai consumato lì dentro. Sono convinto che la tua vicinanza a Vittorio sia *una felicissima combinazione di poesia e crudo realismo*, che se non ha permesso, sicuramente ha favorito la nascita della mia coppia di artisti circensi preferita. Lo ammetto, c'è molta invidia (ma non dirò per chi dei due).

Francesco, avrei dozzine di momenti fra cui scegliere per esprimerti la mia gratitudine, che spaziano dalle occasioni di confronto sul nostro lavoro agli allenamenti in pista al Giuriati. Ce n'è uno però che *già similmente mi stringeva il cuore*, e risale alla mattina in cui mi scoprii escluso dalle borse di studio per i corsi di dottorato, quando, in un clima da *decomposta fiera*, dopo che tutti erano giustamente tornati al *travaglio usato*, venisti alla mia postazione con parole di conforto e di consolazione che sono state fondamentali per riuscire a vivere quella giornata e tutte le successive con una prospettiva di riscatto, anziché di rinuncia, e convincermi che *troverò un modo per riconquistarlo: dopotutto, domani è un altro giorno*. Sei una grande anima, molto più di quello che vorresti dare a vedere.

Michele, nonostante sia foggiano, è una delle persone più solari, disponibili e oneste che conosca. Vado sempre sostenendo che "la vera ricchezza del Minibar sono i nostri clienti", e sono sicuro che finché ci sarà Michele non dovremo mai temere di chiudere bottega. E a costo di scontentare o deludere qualcuno, riconosco qui, pubblicamente, che è lui l'uomo più fresco del LabSAMP (con la meritevole eccezione delle comparsate post-laurea del Re degli Uomini).

Giovanni, l'adeguato alter ego di Michele, giustamente arriva da Vanzago. Mi chiedo come sia stato possibile non rendermi conto che fosse un mio compagno di corso in tutti questi anni. Lo ringrazio per avere fornito, in virtù della sua *forza tranquilla*, una valida copertura, un capro espiatorio ogni volta che il Tesista Mascherato, il misterioso "El Sacco" metteva a segno un colpo: non sarà semplice trovare un alibi quando anche lui completerà il suo percorso.

Monica, la miglior controparte femminile possibile. *Guerre puniche a parte, mi ha accusato di tutto quello che è successo* al LabSAMP, dall'alignment chart che la classificava come chaotic evil all'aver cotto delle uova nel bollitore. *Come pecora muta davanti ai suoi tosatori non voglio belare lamento*, ma solo rendimento di grazie per questa donna straordinaria, una perla rara che ho stupidamente ignorato durante la mia prima vita al Politecnico. Non mi stancherò mai di ascoltarti argomentare su temi in cui la pensiamo in maniera totalmente opposta, sempre sedendomi *dalla parte del torto, perché gli altri posti erano già occupati*: sicuramente ho da imparare più di quanto potrò mai insegnarti.

E questo è un fatto.
Luca, conserverò sempre quella bizzarra ghirlanda variopinta che mi buttasti al collo quella maledetta mattina del 18 luglio, *a date which will live in infamy*, emblematica di quello stile, quell'approccio tipico di uno *che trasforma la giornata in un film di Jean Gabin*. Mi auguro di tutto cuore, prima o poi, che nella mia carriera avrò l'occasione di lavorare con te, perché lasciatelo dire: sei un'altra di quelle persone che unisce un talento cristallino a una straordinaria dedizione al lavoro.
Alessandro, un uomo di una gentilezza fuori dal comune, e un fuoriclasse quando si tratta di VHDL. Nel mio dream team, nel quintetto base del LabSAMP lui, per me, è un titolare inamovibile. Mi vengono in mente almeno un paio di occasioni in cui, dopo avergli esposto un mio problema digitale prima di pranzo, è tornato da me a fine giornata con una soluzione funzionante, quando magari io avevo già cambiato occupazione e quasi mi ero scordato di quello che gli avevo detto. In un mondo di Emanuele Sacchi, di Giulio Gubello e di Diego Barbieri... siate un Alessandro di Tria.
Samuele, il campioncino del LabSAMP. Se è vero che *chi non è capace di ironia è capace di qualunque delitto*, qui siamo in presenza di *un santo, un apostolo*. L'ho sempre sentito particolarmente vicino questo ragazzo, un po' perché dalla sua postazione guarda direttamente verso il mio antro, un po' perché ogni volta che uno dei due ha voglia di fare pausa punta dritto verso la postazione dell'altro, un po' perché è di Bernareggio (ha tutta la mia solidarietà per questo), e sovente frequentiamo gli stessi luoghi. Non vedo l'ora di fare il tifo per te, insieme a Diego, al tuo esordio stagionale con il Botta.
Doctor De Vita, quando sono entrato, il 23 settembre 2021, al LabSAMP, tu eri per me l'unica vera star che conoscessi in quel luogo. Molte altre in seguito hanno illuminato il firmamento che avevo in testa, ovviamente senza scalfire di un solo decimale la tua magnitudine, che è anzi aumentata dopo aver scoperto insieme a Paola della tua rocambolesca scalata nelle graduatorie che ti hanno portato a svolgere qui il tuo dottorato e, come effetto collaterale, a conoscere me. Cosa avrei potuto sognare di più che diventare amico di quello che è il mio idolo?
Arianna, ora ci conosciamo a stento, di vista, e verosimilmente non leggerai mai queste righe, in cui ti prometto che farò tutto il possibile perché tu possa goderti il LabSAMP almeno quanto me lo sto godendo io. Siamo compagni di squadra adesso, e il tuo successo sarà il successo di tutto il laboratorio (l'unico di cui mi importi veramente qualcosa): potrai sempre contare su di me, proprio come io ho sempre potuto contare sulle persone di cui ti ho parlato in queste pagine.

Grazie a tutti voi, per aver reso il LabSAMP quel posto in cui *là dov'è il tuo tesoro, sarà anche il tuo cuore*. E siccome immagino stiate aspettando questa frase da almeno 8 pagine, non mi faccio attendere oltre:

è stato un onore suonare con voi stasera.