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Executive Summary of the Thesis

INTEGRATION OF MONOLITHIC ELECTRONICS IN A STANDARD SILICON PHOTONICS PLATFORM

Laurea Magistrale in Electronics Engineering - Ingegneria Elettronica

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1. Introduction

Silicon Photonics (SiP) is a technology which offers the possibility of integrating multiple photonic devices in a single silicon chip, promising to bring to photonics the same performance and dimensional scaling that has already been experimented in microelectronics. As it is transparent to the Near InfraRed (NIR) wavelengths, Silicon is suitable to be used for the elaboration of the optical signals already employed in long-range fiber optic transmission. In addition, by exploiting the well-known fabrication processes of the CMOS industry, complex SiP circuits made of many optical devices can be integrated in small chips at relatively low costs, developing a new realm of applications and architectures [1].
The silicon-on-insultator (SOI) process allows to implement all the necessary building blocks for creating complex photonics systems, starting from the single waveguide. Its structure is made of a Silicon core and a cladding of SiO_2, as the refractive index difference between the two materials provides a very good confinement of light. Waveguides can then be combined to implement complex photonic devices and consequently photonic systems for optical signal processing.
Silicon has a main drawback though, which is its high sensitivity to temperature variations, that change its refractive index and thus the behaviour of photonic devices. It is therefore required to implement a closed-loop electronic control system, that makes use of multiple sensors and actuators integrated on the SiP chip to ensure its reliable and stable operations. When the complexity of photonic architectures increases, the number of devices to be simultaneously controlled scales accordingly, leading to the need of smart control techniques [2].
In this thesis, the possibility of integrating CMOS electronics directly on photonic chips is explored (Figure 1). This approach allows to significantly reduce the number of electrical connections between the chip and the control electronics, which are becoming a critical bottleneck to further scale the optical complexity.

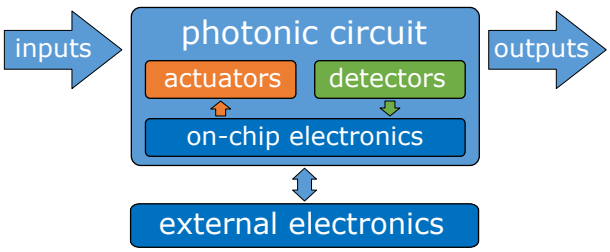

Figure 1: Control scheme of a photonic circuit.

2. Integration of electronic devices in SiP technology

The aim of electronic integration in SiP technology is to implement some processing blocks of the closed-loop control system directly on the photonic chip, thus reducing the complexity and size of the external components. In order not to increase the production cost and allow this approach regardless of the photonic foundry of choice, a zero-change integration of electronic devices and circuits has been investigated, achieved by using only the few essential fabrication steps already available in the photonic technological stack.

The first integrated device is the MOS transistor, which can be then used to create operational amplifiers and multiplexers. As the SOI stack of SiP technologies is optimized to precisely define thin lateral structures but it lacks vertical control of diffusions and self-aligning gate process, lateral gate MOS transistors were designed. Both n- and p-type MOSFETS were realized with the same geometry, simply by changing the doping species of the diffusion regions, by exploiting the fact that the native silicon layer of photonic chip is naturally depleted of carriers to achieve a reasonably low threshold voltage. Both devices have been electrically characterized and can be used to realize functional electronic circuits (Figure 2).

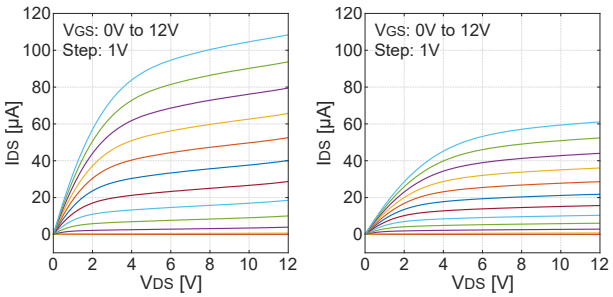

Figure 2: Charactertistic curves of an nMOS and a pMOS transistor, respectively.

The possibility of implementing a BJT was studied as well. A *npin* device was realized and characterized (Figure 3), with a circular and lateral structure similar to the one employed in standard CMOS technologies, in order to maximise its current gain $\beta = I_C/I_B$. The results are promising, as a β around 30 is obtained, an order of magnitude greater than what reported in

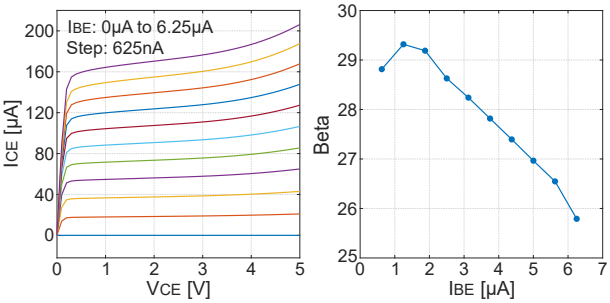

Figure 3: Characteristic curves of an npin BJT.

other studies [3]. The device can be used in low-noise amplifiers or low-impedance output driving stages.

Since the transistors performance was well validated, SiP MOSFETS have been used to implement CMOS logic gates and analog switches. Firstly, a CMOS inverter has been designed, made of one nMOS and one pMOS. Considering that the capacitive load it drives is in the order of few fF, its small current does not limit the switching speed. Results show that the logic gate has good performance for both $5\,V$ and $12\,V$ power supply (Figure 4). The same is true for the 2-input NOR port subsequently realized, which also features an inverter at its output in order to make an OR gate too. The difference between the NOR and OR outputs, the latter being steeper, shows the ability of the digital circuit to restore the edges even in this unconventional technology.

Single-Pole-Double-Throw (SPDT) switches were also implemented as building block for multiplexing circuits, using 2 pass-transistors driven in opposite phase. Each transistor is made of 16 nMOSFET in parallel and the resulting R_{ON} is $1.8\,k\Omega$ for $V_{GS} = 12\,V$ while R_{OFF} is $2\,G\Omega$ for $V_{GS} = 0\,V$. Their bandwidth is around $100\,MHz$, suitable for the intended application.

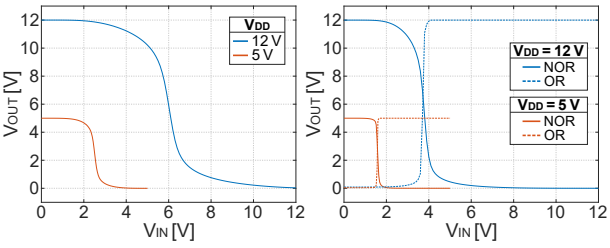

Figure 4: Input-output characteristic curves of the inverter and the NOR/OR gate.

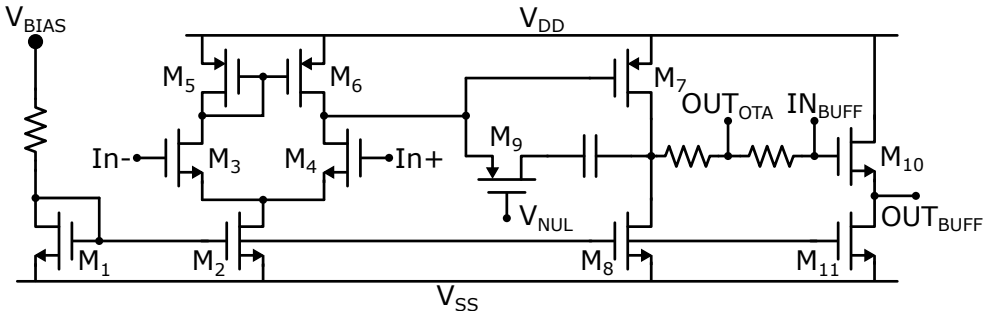

Figure 5: Schematic of the operational transconductance amplifier.

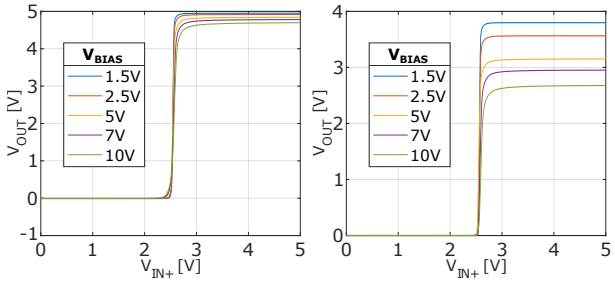

Figure 6: Characteristic curves of the amplifier before and after the buffer, respectively.

3. Operational Amplifier in SiP technology

A possible application of the realized MOSFETs is the design of an operational amplifier. It would allow, for instance, to implement an on-chip transimpedance amplifier (TIA) for photodiodes readout, allowing to transmit to the external electronics a voltage instead of a current. It could also be used to create a simple Sigma-Delta converter, to convert analog signals into digital ones without leaving the photonic chip.
The circuit was designed as a standard 2-stage operational transconductance amplifier (OTA), with a differential input stage and a current mirror load followed by a second gain stage and a Miller compensation (Figure 5). A class A source follower has been included as output buffer. The V_{BIAS} terminal has voluntarily been split from V_{DD} so to freely change the circuit current bias and optimize its gain. As for the layout, the common centroid technique was used to place the different transistors, to minimize the effect of fabrication mismatches.
The sizing process was done without simulations, since the employed transistors do not have a functional behavioural model. A single transistor of each type has thus been characterized in the final working conditions, allowing to choose the number of MOSFETS in parallel to obtain the desired characteristics. The estimated values are $G = 79.77$ and $GBWP = 2.31\,MHz$, for $V_{DD} = 5\,V$ and $V_{BIAS} = 5\,V$.
The device was characterized at different bias conditions to assess the open-loop transfer function, by sweeping the non-inverting input while keeping the inverting one at $2.5\,V$ (Figure 6). As in theory, the DC gain is higher for lower bias voltages, since it follows the equation:

$$G_{MAX} = g_m \cdot r_0 \propto \sqrt{I} \cdot \frac{1}{I} = \frac{1}{\sqrt{I}}.$$

For $V_{BIAS} = 5\,V$, $G = 69.79$ at the OTA output, only 12% lower than the design specification.
Finally, the behaviour of the circuit as a function of the input frequency has been assessed. Its transfer function was measured in a buffer configuration at different V_{BIAS}, to evaluate the circuit's bandwidth (Figure 7). As expected, it is smaller for lower bias voltages, confirming the tradeoff between gain and speed. For $V_{BIAS} = 5\,V$, $BW = 1.9\,MHz$ is obtained, close to the expected value.

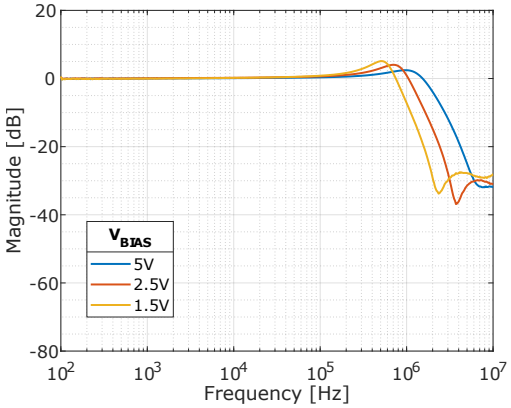

Figure 7: Transfer function of the amplifier in buffer configuration.

4. Time-multiplexed control of SiP circuits

The designed transistors have been used also to design an analog multiplexer (MUX), a key element for electronic control of high density optical systems. In standard conditions, the number of electrical connections between photonic chip and external electronics scales linearly with the number of photonic devices, limiting the scalability of the approach. A possible solution to this issue is to multiplex in time the readout and driving of sensors and actuators. This approach can be effectively employed since photodiodes and actuators work at relatively low frequency, to compensate temperature drifts happening with a *ms* time scale.

A 16-inputs-1-output MUX has already been monolithically integrated on a single photonic chip for time-multiplexed readout of on-chip photodiodes, by using around 1000 transistors. With this setup, the number of electrical connections required for readout to operate a photonic chip scales as:

$$N_{CONN} = \log_2(N_{PD}) + 5.$$

This number must be compared to N_{PD} in the case on parallel readout without MUX. It is clear that this solution is convenient for a number of sensors greater than 8, the improvement becoming larger and more evident as the number of sensors increases.

In order to further reduce the total number of connections, an architecture for time-multiplexing of actuators has been developed. It is indeed required since the number of sensors and actuators on a photonic chip is similar. The multiplexer structure is the same used for the PDs, connected to nMOS transistors in a source follower configuration to drive the actuators (Figure 8). In this way, the MUX does not need to provide any current to the actuators, allowing to store the driving voltage on a 10 pF on-chip memory capacitance connected to the MOSFET gates. As for the PDs, the MUX allows to reduce the number of connections required to operate the photonic chip with a logarithmic proportionality, therefore it is particularly advantageous in large-scale circuits.

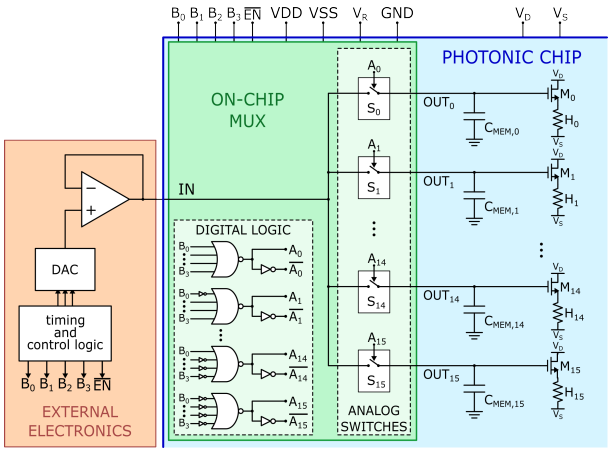

Figure 8: Scheme of the multiplexer.

The multiplexer has been electrically characterized. Its ON and OFF resistances are the same measured for the switches in Section 2, certifying that the MUX properly connects and disconnects the input and the output depending on the digital code. Similarly, the device signal bandwidth is $100\,MHz$. The settling time of the MUX was calculated by measuring the transient that occurs when changing the configuration of the digital bits (Figure 9).

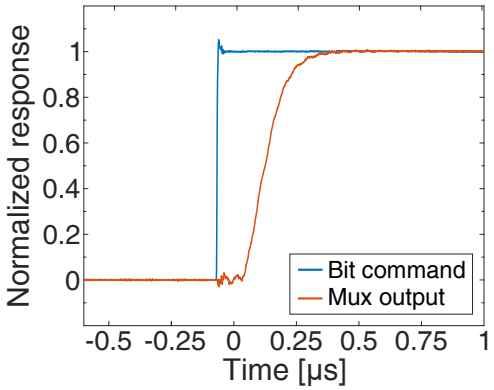

Figure 9: Transient of the multiplexer.

It is equal to $500\,ns$, corresponding to a maximum switching frequency of $f_{MUX} = 2\,MHz$. At last, the times required to charge and discharge the memory capacitor were evaluated. An update time constant of $40\,ns$ was found, much shorter than the heater reponse time, certifying that the MUX does not limit the performance of the photonic circuit. The discharge rate, instead, leads to a minimum refresh frequency equal to $f_C = 1\,kHz$. The ratio of switching and refresh frequencies determines the maximum number of channels that can be multiplexed without pnalties in the optical performance, which results to be $N_{CH_{MAX}} = f_{MUX}/f_C = 2000$.

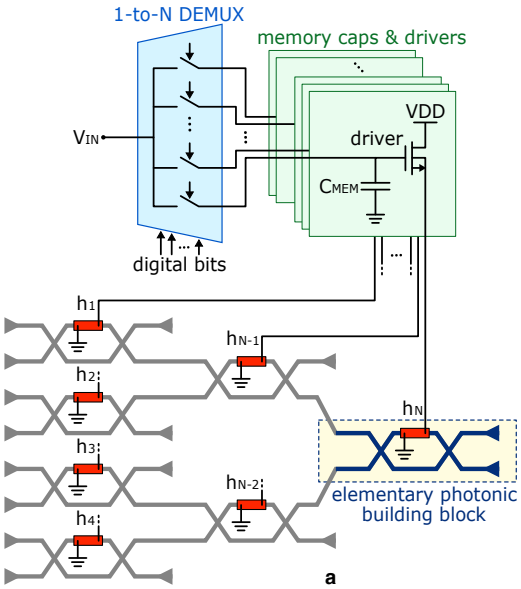

Figure 10: Scheme of the optical circuit.

5. The optical circuit and its interface board

The optical circuit employed to test the multiplexing of actuators is a mesh of 15 Mach-Zehnder Interferometers (MZI) arranged in a tree-like structure (Figure 10). The aim of the circuit is to route light from each of the inputs to a single optical output. Each MZI requires a heater and a PD to be operated, for an overall number of 15 sensors and actuators that need to be time-multiplexed to control the chip [4].
The photonic chip needs to be complemented by external electronics to work properly. An interface board containing the circuitry needed to operate the MUXes and read the PDs has been designed, connected to a larger board performing the feedback control action (Figure 11). The board has been shaped to allow easy light coupling to the chip with optical fibers.

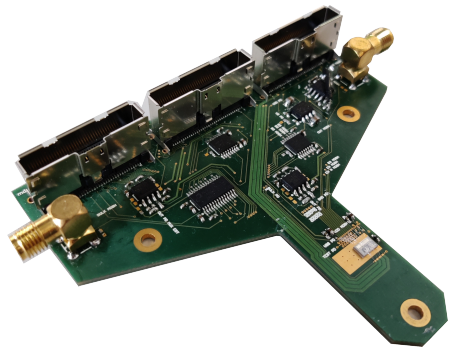

Figure 11: Photo of the interface board.

6. Optical characterization of the multiplexing of actuators

The optical functionality with time-multiplexed actuators was finally validated. In order to do that, it was first mandatory to ensure that the on-chip source followers can properly drive the heaters and control the optical power at the output of each MZI. A single driver was first tested, by sweeping its gate voltage. An input beam of constant intensity has been injected in the MZI and the output has been monitored with a bench-top photodiode to evaluate the operation of the circuit. Figure 12 shows the output of the power monitor and the power dissipated by the heater as a function of the follower gate voltage.

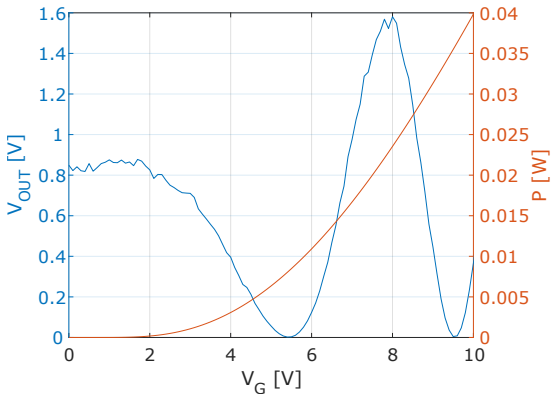

Figure 12: Source follower characterization.

The circuit is able to provide up to 10 mA current to the actuator, resulting into a maximum dissipated power of 40 mW. This translates into a shift of the sinusoidal MZI transfer function of more than one period. An efficiency of $27\,mW$ to achieve a full 2π phase shift can be derived from the measurement. The driver can thus be used to effectively control the optical device and precisely set the amount of power at its output. Then, the optical performance when multiplexing the actuator of a MZI has been assessed. The disable pin of the MUX, which disconnects all the outputs from the input when asserted, has been driven with a square wave, to assess the effect of the memory capacitor discharge on the optical output. The measurement was repeated at different switching frequencies between 0.1 Hz and 1 MHz (Figure 13). At low frequency, below $10\,Hz$, a relevant discharge of the memory capacitor was observed, resulting in a significant change of the MZI operating point. Instead, when the driver is operated with a refresh

rate above $100\,Hz$, a negligible power variation of $0.03\,dB$ is measured, thus ensuring that the circuit can keep the heater current constant even when time-multiplexing is enabled.
Lastly, the impact of the multiplexed control on the transmission of modulated signals was checked. A cascade of 2 MZI was used for the test (Figure 14). A $10\,Gb/s$ optical signal was split, decorrelated and coupled to the 2 inputs of the circuit, generating a reference and an interference signal. The impact of the interference was minimized by correctly driving the actuator on the first MZI, then the disable bit was activated at different switching frequencies. As expected, if the switching frequency is too low the capacitor is significantly discharged, letting the interference reach the output and degrade transmission. Instead, when the frequency is increased, the impact of interference is minimized to the same level observed when the heater is driven continuously. The measurement thus certifies that the time-multiplexed approach can be applied to the actators without penalties in the optical performance even at high data-rates.

7. Conclusions

Monolithic integration of active electronics on a Silicon Photonics chip for the of control large-scale optical systems has been explored in this thesis. The designed devices and circuits have been implemented without changing the standard fabrication processes of the technology, in a zero-change approach.
After characterizing the CMOS transistors, a full operational amplifier has been designed and measured. It can be used to integrate analog circuits on the photonic chip, as TIAs for readout of photodiodes or analog-to-digital converters. The performance of the amplifier can be further improved based on the acquired experience, to the point of being able to move the whole control systems on the photonic chip itself.
A multiplexer for sequential control of on-chip actuators has also been successfully characterized. It can be used to drive up to 2000 actuators using few electrical signals, without degrading the optical performance. The performance of the device will allow to demonstrate sequential control of a large-scale circuit, where both readout and actuation are multiplexed in time.

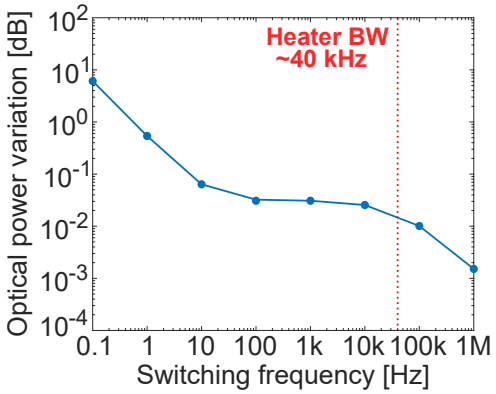

Figure 13: Optical power variation as function of the MUX switching frequency.

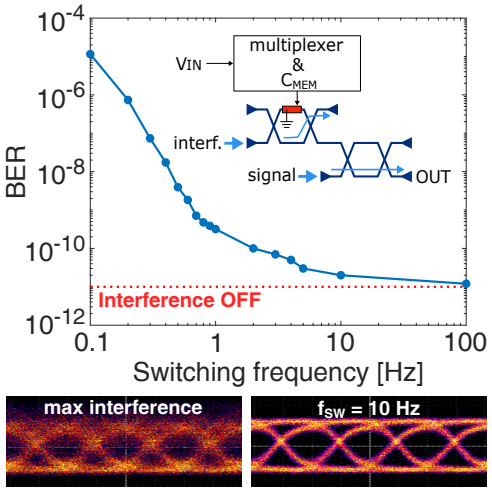

Figure 14: Bit Error Rate and eye diagram when the actuators are time-multiplexed.

References

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