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Design of a Testing system for a 83-channel SDD front-end board

Tesi di Laurea Magistrale in
Electronics Engineering - Ingegneria Elettronica

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Abstract

Sterile neutrinos are a minimal extension of the standard model of particle physics. A promising model-independent way to search for sterile neutrinos is via high-precision β-spectroscopy [13]. The Tritium Laboratory Karlsruhe (TLK) provides an intense $10^{11} B_q$ gaseous tritium source.To handle exceedingly high rate and to maintain excellent spectroscopic properties at the same time, an energy resolution of 300 eV FWHM at 20 keV with a multi-pixel silicon drift detector (SDD) and a readout system are currently being developed in the TRISTAN project.The single acquisition system module is made of two boards hosting the ASICs with the charge sensitive amplifiers (CSA) and with a total of 83 CSA channels per board. Then biasing and Data AcQuisition system (DAQ) are used respectively to bias the detector and to filter and collect the events signal coming from the SDD. Such a system will be finally implemented in 21 modules that require 1 year of measurement reliability. The testing board developed in this thesis allows to check the functioning property of the ASIC board in the acquisition system that, because of its high density of channel and wire bonding, has a significant probability to have manufacturing problems that are visible only through board testing. This allows to save a lot of time during the verification of the correct behaviour of all the acquisition systems before the mounting of all the 21 modules.

Keywords: Dark Matter, Kev Sterile Neutrino, Katrin experiment, Tristan experiment,SDD, CSA, MicroController, Python GUI, PCB, testing board

Sommario (Abstract in Italian)

Il neutrino sterile caratterizza una estensione del modello standard nella fisica delle particelle. Una ricerca del neutrino sterile, che non sfrutta modelli, utilizza la spettroscopia ad alta precisione del decadimento beta. Il laboratorio TLK a Karlsruhe può fornire un'intensa sorgente gassosa di trizio che produce $10^{11} B_q$. Per poter gestire flussi incredibilmente alti ed allo stesso tempo mantenere eccellenti proprietà spettroscopiche, per il progetto Tristan, è stato necessario implementare dei rivelatori (SDD) con una risoluzione di 300eV(FWHM)@20KeV ed un sistema di acquisizione per il segnale che viene prodotto dopo ogni evento. Un singolo modulo del sistema di acquisizione è composto da una scheda che contiene gli ASIC con gli amplificatori di carica (CSA) per gli SDD (83 canali disponibili). Inoltre sono presenti un sistema di polarizzazione del rivelatore ed un altro per l'elaborazione del segnale generato dopo un evento (elettrone colpisce il rivelatore). Nel progetto finale il singolo modulo verrà implementato in una matrice di 21 moduli che richiederà una affidabilità di funzionamento che possa durare per almeno l'anno di utilizzo del sistema. La scheda di test, sviluppata nell'ambito di questa tesi, permette di verificare il corretto funzionamento della scheda che ospita gli ASIC. A causa dell'alta densità di linee e connessioni con fili volanti, per gli 83 canali degli ASIC c'è un'alta probabilità che sia presente qualche errore di produzione, identificabile solo con il test della scheda. Prima che l'intero modulo venga assemblato, tutti i componenti devono essere testati e la scheda di test permetterebbe di risparmiare molto tempo.

Parole chiave: Materia Oscura, Neutrino Sterile nei Kev, esperimento Katrin, esperimento Tristan ,SDD, Amplificatore di carica (CSA), MicroControllore, GUI in Python, circuito stampato (PCB), schede di test

Contents

Introduction

This thesis introduces the neutrino physics and the dark matter. Subsequently a relation between the two is given because that great discoveries on the nature of the neutrino could provide a viable Dark Matter candidate with a minimal extension of the standard model via creation of KeV-sterile neutrino. Then the KATRIN apparatus and experiment is described in details to allow the comprehension of its great capability. In fact the Tritium Laboratory Karlsruhe (TLK) is able to supply an intense 10^{11} B_q gaseous tritium source while the electromagnetic spectrometer technique provide sub-eV energy discrimination, obtaining the ability to precisely measure the β-decay spectrum, grants sensitivity to additional physics topics such as sterile neutrinos. Now TRISTAN is at the center of the KATRIN experiment evolution. By complementing the high β-decay capability of the KATRIN apparatus, in 1 year of KATRIN and TRISTAN detector module operation at full source strength,it can bring a statistical sensitivity (of the mixing amplitude $\sin^2\theta$ of the sterile neutrino with the active Standard Model electron neutrino) of the order of $\sin^2\theta = 10^{-8}$.

After all the theoretical discussion on the neutrinos and different advanced engineering apparatus in the KATRIN beamline, the Discussion focuses on the acquisition system developed for the TRISTAN project. The first and main component is the Silicon Drift Detector (SDD) developed in multi-pixel configuration. The different steps for the development of the final 21 166-pixel detector modules, start by presenting the first 1-pixel SDD characterisation with fast electrons (with a SEM). Then the various prototype with 7, 12, 47 and finally 166 are described with their relative characterisation and testing setups. Furthermore, since the thesis focuses on a board that tests one part of the detector acquisition system, a deeper discussion is made on the development and changes occurred for the different components that make up the whole system. First, the ETTORE ASIC is used in the amplification stage of the signal coming from the detector and the ASIC boards was developed to host it. Second, the biasing systems id used in the different levels of the Detector evolution and lastly, you will find a brief discussion on the DAQs used.

The final part focuses on the main topic of the thesis, the Testing board. This board has been developed to test the ASIC board behaviour. The uncertainties on ETTORE

(ASIC) board are given by its high density of channel and bonding wires that could give some problems, during the production and the mounting, that are not immediately visible. The testing board is a 6 layers PCB with USB connection power connection and a μC that handles all the test and the selection of the channels of the ASICs. To allow a user to read the result and choose what kind of test to do and for which set of channels, a Graphic User Interface (GUI) was developed with the python-tkinter module.
Finally, the future developments of the TRISTAN system are recalled. For the testing board future, the modification to accommodate new tests. Since the board is not working properly yet, some solutions are presented. For example, one of the possible changes to solve the problems of the board, could be to decrease the testing velocity. In the end the 40-pin ribbon connector on the testing board is presented as the starting point for the development of Extension (slave) testing boards to check on other, sensitive to production processes, parts of the acquisition system.

Overview of the chapters

1. **TRISTAN Project :**
   It is divided in 3 `sections`. The first discusses about the neutrino physics and its relation with dark matter. Then the second section mention the KATRIN project as a fundamental base from which the TRISTAN project is born and developed. Some of the KATRIN experiment are described in a general way. Finally, in the last section the TRISTAN project is explained in details.

2. **Acquisition System and testing board :**
   It is divided is 4 `sections`. The first section talks about the `Silicon Drift Detector` (`SDD`) used for the acquisition of the electron arriving from the KATRIN apparatus and describes the evolution of its size and technology for the TRISTAN project. The second section contains the ETTORE board history and some specifics on the ETTORE ASIC. The third section discusses the evolution of the Bias board used in the different setups for the different sizes of detector. The last section describes ATHENA&Kerneros versus CAEN DAQs and introduces briefly the older DANTE DAQ.

3. **Testing Board and Gui for the ETTORE board:**
   It is divided is 6 `sections`. The first talks about a general description of a testing setup for the ETTORE board connected to the Testing board with some details on

the delicate step of the setup. Then the second section describes in details the testing board with a focus on the component used and the function that are implemented. Following, in the third section, a detailed description of the GUI for the testing board, is given. The fourth section describes how the testing board and the GUI are working together, by explaining how the communication protocol works. The fifth section describes in a schematic way the testing circuit functions and what are the expected results. Finally, the sixth and last section presents the setup for the characterization of the testing board. Some of the testing results are presented and discussed.

1 | TRISTAN project

1.1. The NEUTRINOs physic and DARK MATTER

There are three types of neutrinos discovered: it is a well-established experimental fact that the neutrinos and antineutrinos are leptons of three varieties (types) or flavours: electron, νe and $\bar{\nu}$e, muon, $\nu\mu$ and $\bar{\nu}\mu$, and tauon, $\nu\tau$ and $\bar{\nu}\tau$ (1.1).

Figure 1.1: The different types of neutrino.

Since they have no electrical or strong charge, neutrinos almost never interact with any other particles. Most neutrinos pass right through the Earth without ever interacting with a single one of its atom.
Neutrinos are produced in a variety of interactions, especially in particle decays. In fact, it was through a careful study of radioactive decays that physicists hypothesized neutrino's existence.

For example:

1. In a radioactive nucleus, a neutron at rest (zero momentum) decays, releasing a proton and an electron.
2. Because of the law of conservation of momentum, the resulting products of the decay must have a total momentum of zero, which the observed proton and electron clearly do not. (Furthermore, if there are only two decay products, they must come out back-to-back.)
3. Therefore, we need to infer the presence of another particle with appropriate momentum to balance the event.
4. The hypothesis of antineutrino was released; experiments have confirmed that this is indeed what happens.

Because neutrinos were produced in great abundance in the early universe and rarely interact with matter, there are a lot of them in the Universe. Their tiny mass but huge numbers may contribute to total mass of the universe and affect its expansion.(From `Particle Adventure` site: [15])

The tiny mass of neutrino makes the neutrino one of the most interesting particles, one that might hold the key to physics beyond the Standard Model. With a mass at least six orders of magnitudes smaller than the mass of an electron, but non-zero, neutrinos leads to great challenges in its experimental determination. Three approaches are currently pursued: an indirect neutrino mass determination via cosmological observables, the search for neutrinoless double β-decay, and a direct measurement based on the kinematics of single β-decay. The Karlsruhe Tritium Neutrino (KATRIN) experiment is a large-scale tritium-β-decay experiment. It is currently being commissioned at the Karlsruhe Institute of Technology, Germany. KATRIN is designed to achieve a neutrino mass sensitivity of 200 meV after 3 full-beam years of measurement time. (Direct Neutrino Mass Experiments, 2016, S. Mertens [12])

Now, talking about Dark Matter, is possible to say that: the majority of the Universe may not be made of the same type of matter as the Earth. We infer from gravitational effects the presence of this Dark Matter, a type of matter that we cannot see. (From `Particle Adventure` site: [14]). Dark Matter is a hypothetical form of matter that is thought to account for about 85% of the total `Mass` in the universe. According to the Planck mission's cosmic microwave back-ground data, we have an estimation of the com-

position of the Universe: ordinary matter (4.8%), neutrinos (0.1%), cold dark matter (26.8%), and dark energy (68.3%) [17] (1.2).

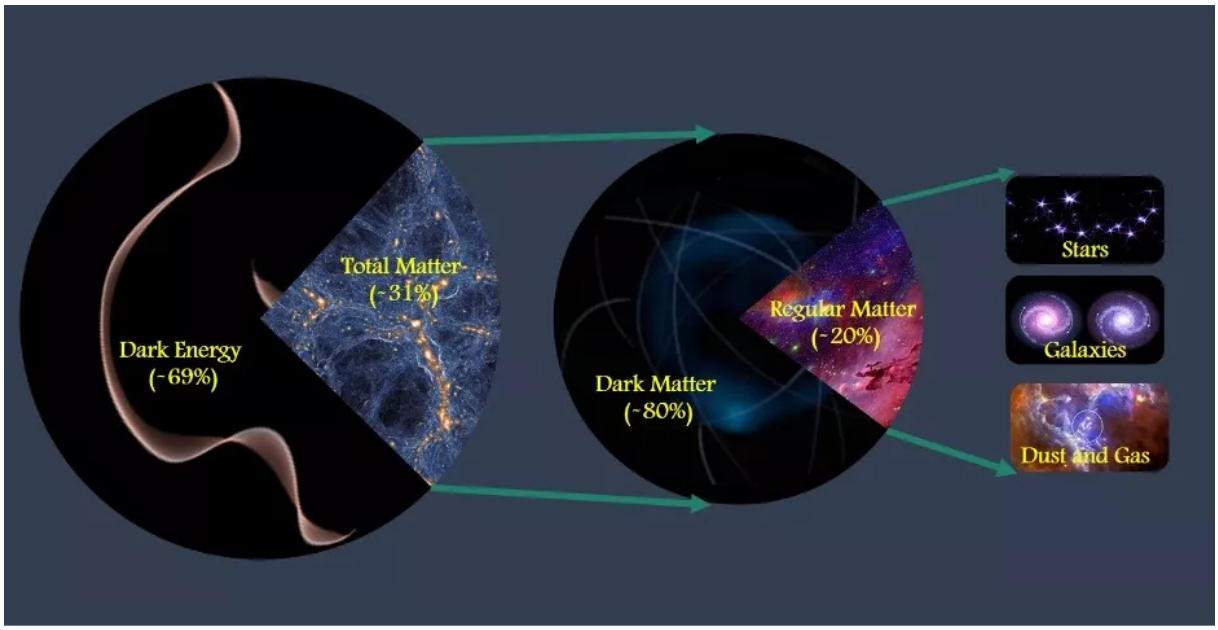


Figure 1.2: The universe composition.

It is called dark because it interact only through gravitational effects. It is therefore not directly observable, and it has been theorized to account for discrepancies between experimental observations and the current laws of physics, hence its detection is extremely difficult. Its presence can explain some astrophysical observations, like gravitational effects that cannot be explained unless more matter than what can be seen is present. The candidate particle for the dark matter composition must be, for obvious motivations, some new kind and it must be included in the weakly interacting massive particles.

`how can we find out if neutrinos are part of the dark matter?`
Great discoveries on the nature of the neutrino have been brought to light by solving experimental anomalies. If we know now that out of three mass eigenstates, two of them must be non-zero, the mechanism generating the neutrino mass is still pending. Most hypotheses need to invoke the right-handed partner of the already observed left-handed active neutrino. This approach could provide a viable Dark Matter candidate with a minimal extension of the standard model via creation of **KeV-sterile neutrino** (1.1). The mass-range of this sterile neutrino sweeps along several orders of magnitude. Nuclear physics, astrophysics and cosmology all provide constraints on the mixing angle of such a

particle. The TRISTAN project focuses on the 1-20 keV sterile neutrino candidates where the boundary imposed by astrophysics on the sterile-active mixing angle θ is on the order of $\sin^2\theta < 10^{-6}$ [10].

1.2. KATRIN experiments

KATRIN probes the neutrino mass via a precise measurement of the electron energy spectrum resulting from the β-decay of molecular tritium:

$$T_2 - - >^3 HeT^+ + e^- + \bar{\nu}_e, \tag{1.1}$$

The nonzero rest mass of the neutrino results in a distortion of the β spectrum that is statistically most significant at the endpoint of the spectrum. This shape distortion grants sensitivity to the square of the effective neutrino mass

$$m_\nu^2 = \sum_i |U_{ei}|^2 * m_i^2 = m_\beta^2, \tag{1.2}$$

An incoherent sum of the distinct neutrino-mass values is weighted by their contributions to the electron-flavor state, given by the elements Uei of the Pontecorvo-Maki-Nakagawa-Sakata (PMNS) matrix. Here, the observable m_ν is denoted, but m_β is often used for the same observable in the literature.
Only about one part in 10^{13} of the β-decays appears in the last eV of the spectrum; a statistically significant measurement at the endpoint of the spectrum therefore requires an extremely bright source and excellent resolution for measuring the energy of the decay electron. The Tritium Laboratory Karlsruhe (TLK) provides an intense 10^{11} Bq gaseous tritium source while the electromagnetic spectrometer technique provide sub-eV energy discrimination. The ability to precisely measure the β-decay spectrum grants sensitivity to additional physics topics such as sterile neutrinos, the number density of relic neutrinos and Lorentz-invariance violation [3].

1.2.1. KATRIN apparatus

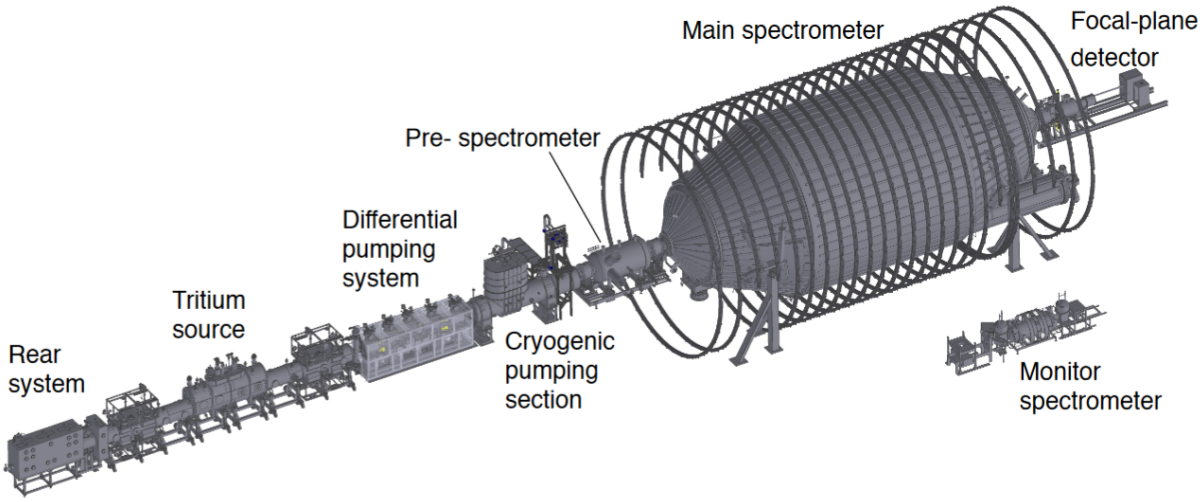


Figure 1.3: design view of the complete KATRIN apparatus [3].

The 70 m KATRIN beamline is designed to perform high-precision energy analysis of β electrons from a high-luminosity, gaseous T_2 source. T_2 gas is purified in a tritium loop system, which continuously delivers cold T_2 gas to the center of the source system. The gas diffuses to both ends of the source-system cryostat, where the first pumping stages are located. A fraction of the T_2 molecules experiences β-decay during their flight within the source beam tube. Of the resulting β_s, those that are emitted in the downstream direction are guided by magnetic field lines through the chicanes of two consecutive pumping stages that together reduce the flow of neutral tritium by some 14 orders of magnitude. The first, differential pumping stage relies on turbomolecular pumps, while the second is a cryogenic pumping stage in which tritium is adsorbed onto an Ar frost layer that lines the beam tube.

Past the pumping systems, the β_s reach a pair of tandem spectrometers designed according to the principle of magnetic adiabatic collimation with electrostatic filtering (MAC-E filters). A MAC-E filter uses magnetic-field gradients to collimate the β-electron flux, allowing a longitudinal retarding potential U to set a threshold on the total kinetic energy of the β_s. A β with energy $E > qU$, where q is the electron charge, will pass through the spectrometer to the downstream exit; if $E < qU$, the electron cannot pass and is instead reflected in the upstream direction [3].

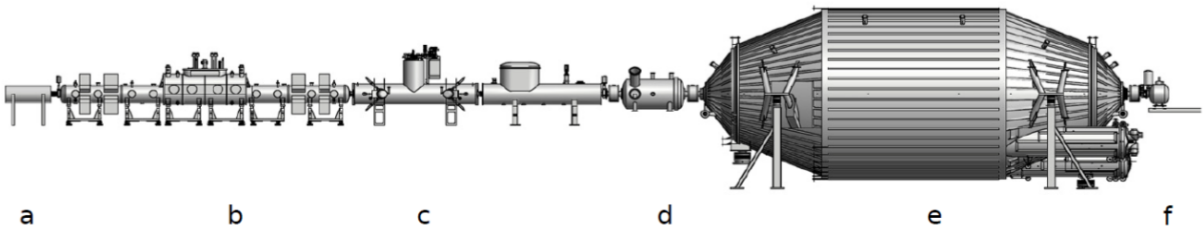


Figure 1.4: Section view of the KATRIN beamline module with a) the Rear Section for diagnostics, b) the windowless gaseous tritium source WGTS, c) the pumping section with the DPS and CPS cryostats, and a tandem set-up of two MAC-E- filters: d) the smaller pre-spectrometer and e) the larger main spectrometer with its surrounding aircoil system. This system transmits only the highest-energy β-decay electrons onto f) the solid-state detector where they are counted [2].

- **a) The Rear Section for diagnostics:**
  A gold plate which acts as the reference potential for all electrodes, is installed. Moreover, the rear section is equipped with a calibration e-gun and other diagnostic tools [11].
  e.g. : Behind the rear wall, silicon drift detectors monitor the source activity by detecting X-rays from β interactions in the rear wall. An electron gun provides calibration electrons with controlled angle and energy; these electrons enter the source via a small aperture in the center of the rear wall, and travel the entire length of the beamline [3].

- **b) The windowless gaseous tritium source (WGTS):**
  Gaseous tritium, with high isotopic purity ($> 95\%$) from a pressure-controlled buffer vessel is continuously injected at 30 K into the WGTS at the midpoint of its 90 mm diameter, 10 m long stainless steel beamtube [2].

- **c) The pumping section with the differential (DPS) and cryogenic (CPS) pumping section:**
  Then the gas diffuses to both ends where it is pumped out by a series of turbomolecular pumps (TMPs) in the DPS, yielding the nominal column density of $\rho = 5{*}10^{17}\frac{molecules}{cm^2}$ (resulting in an activity of molecular tritium decays with $10^{11}B_q$), In combination with the CPS, housing a large-capacity cryotrap operated at around 3 K. *(Note, Becquerel (Bq) is: 1 Bq = 1 disintegration per second (dps))*. The source magnetic field as well as other superconducting solenoids adiabatically guide

primary β-decay electrons, secondary electrons, and ions to the spectrometers. A series of blocking and dipole electrodes eliminates ions by an $\boldsymbol{E} \times \boldsymbol{B}$ drift to the beam-tube, so that they cannot generate background in the spectrometer section [2].

The tandem configuration of MAC-E-filters performs a two-step filter process:

- **d) The smaller pre-spectrometer :**
  It was operated at fixed high voltage (HV) of $-10.4kV$ and works as a pre-filter to reject electrons that carry no information on m_ν [2]. However, following the discovery that tandem spectrometer operation led to an effectively energy-dependent background, KATRIN now runs without energizing the pre-spectrometer. β electrons with sufficient energy pass through the main spectrometer and are counted in the focal-plane detector [3].

- **e) The larger main spectrometer with its surrounding aircoil system. This system transmits only the highest-energy β-decay electrons**
  Variable qU is applied to the main spectrometer for precision filtering of β-decay electrons close to E_0. Its huge size guarantees fully adiabatic motion to the central "analyzing plane", where the minimum magnetic field B_{min} and the maximum retarding energy qU coincide for the filtering process to occur [2].
  (Note : A defining property of a MAC-E-filter is $\Delta E/E$, the filter ***width*** *at energy E, which is given by the ratio Bmin/Bmax of the minimum to maximum magnetic field in non-relativistic approximation. Until September 2019 the ratio $\frac{0.63mT}{4.24T}$ was equivalent to $\Delta E = 2.8\ eV$ at E_0 [2].)*

- **f) The solid-state detector where they are counted**
  It is the focal-plane detector, a monolithic silicon p-i-n diode segmented into 148 equal-area pixels. A 10 kV post-acceleration electrode, immediately upstream of the detector, elevates the signal energies above local backgrounds [3].

1.2.2. How is the TRISTAN project enhancing the KATRIN experiment?

For higher-statistics measurements, a new detector system for KATRIN is under development(TRISTAN project) 1.5.

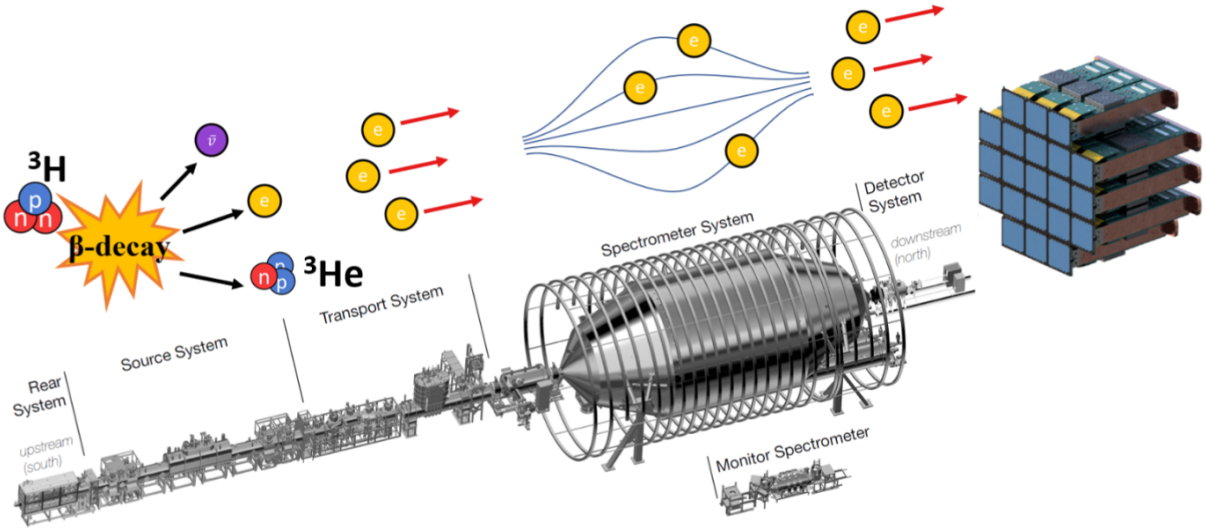


Figure 1.5: Design view of the complete KATRIN apparatus with TRISTAN detector module on the right and drawn description of the β-decay energy electron path through Katrin [11].

With 1 year of KATRIN and TRISTAN detector module operation at full source strength, a statistical sensitivity of the order of $\sin^2\theta = 10^{-8}$ can be reached. It is, however, extremely challenging to control systematic uncertainties at this level. Therefore, the targeted design sensitivity is $\sin^2\theta = 10^{-6}$, which would surpass the sensitivity of previous laboratory-based, searches and reach a region of cosmological interest. Note that while astrophysical constraints on the mixing are quite strong, there are ways to evade them and to bring the mixing up to scales reachable by the TRISTAN detector upgrade. Figure 1.6 shows the sensitivity for different measurement scenarios, using the KATRIN apparatus with the TRISTAN detector to search for sterile neutrino [3].

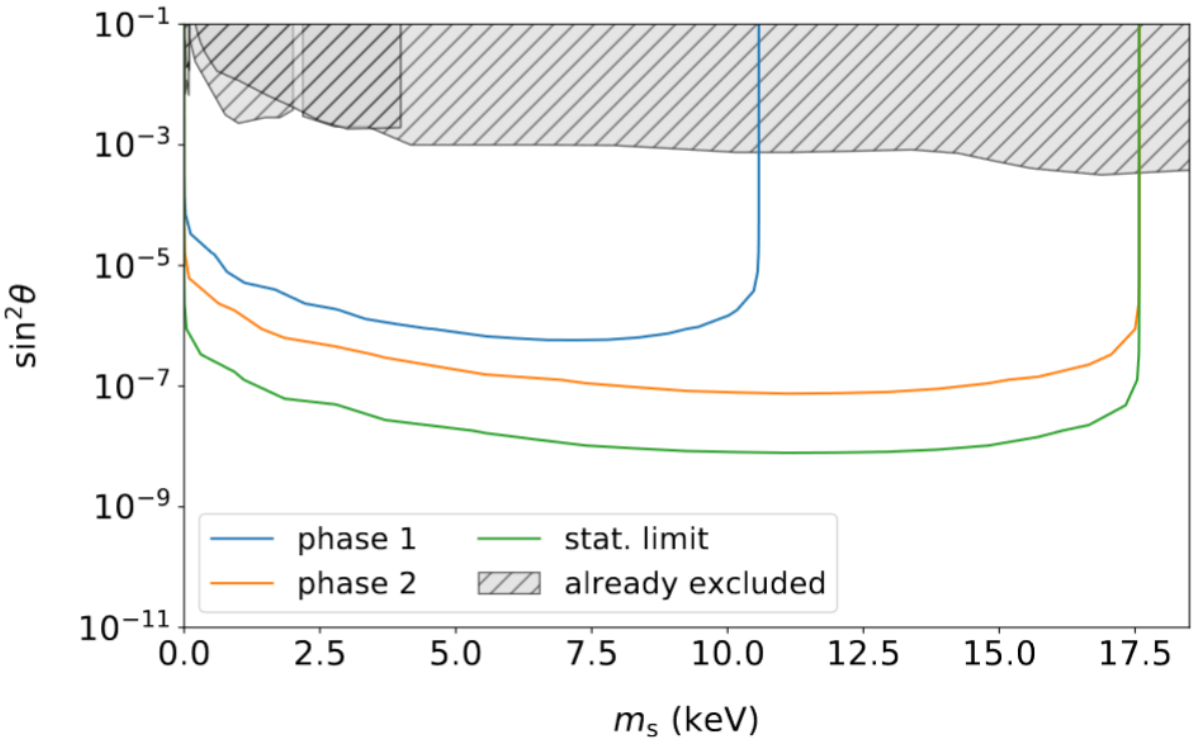


Figure 1.6: KATRIN sensitivity to keV-scale sterile neutrinos in different scenarios. The statistical limit assumes 10^{18} electrons over the full energy range, corresponding to a measurement time of one year at the full KATRIN source strength. **Phase 1** denotes the first stage of TRISTAN operation with a reduced amount of TRISTAN modules (approx. 1000 pixels) and a lowered KATRIN source strength (0.3% of the nominal column density). The spectrum is scanned on an energy interval of 8 keV to 18 keV with a total measurement time of $t_{meas} = 0.5yrs$. In the follow up stage **(phase 2)**, the TRISTAN detector is operated with all 3500 pixels. The tritium spectrum is scanned on the full energy range at a reduced source activity of 2% of the nominal column density for $t_{meas} = 1.0yrs$ [3].

1.3. TRISTAN experiment

I have introduced the TRISTAN project before in the Sec.1.2 by describing it as a complementary part for the KATRIN project. I already said that the project consist in the use of a new kind of detector 1.5, the Silicon Drift Detector (consequently even a new acquisition system for the new SDD has been developed). The final purposes of the TRISTAN project is presented here.

Note on the sterile neutrino at the KeV scale:
Because the β-decay spectrum is given as a superposition of the spectra corresponding to each mass eigenstate $m(\nu_i)$, weighted by its mixing amplitude $|U_{ei}|$ to the electron flavor and since the mass splittings between the three light mass eigenstates are so small, no current β-decay experiment can resolve them. Instead, a single effective light neutrino mass $m^2(\nu_e) = \Sigma_{i=1}^{3}|U_{ei}|^2 m^2(\nu_i)$ is assumed. If the electron neutrino contains an admixture of a neutrino mass eigenstate with a mass m_s (sterile neutrino) in the keV range, the different mass eigenstates will no longer form one effective neutrino mass term. In this case, due to the large mass splitting, the superposition of the β-decay spectra corresponding to the light effective mass term $m(\nu_e)$ and the heavy mass eigenstate m_s can be detectable. The differential spectrum can be written as

$$\frac{d\Gamma}{dE} = \cos^2\theta \frac{d\Gamma}{dE}(m(\nu_e)) + \sin^2\theta \frac{d\Gamma}{dE}(m(\nu_s)), \tag{1.3}$$

where θ describes the active-sterile neutrino mixing and predominantly determines the size of the effect on the spectral shape. Figure 1.7 shows a qualitative example with perfect energy resolution and no energy smearing from atomic, thermal or scattering effects [1].

Since the sterile neutrino mass is unconstrained, the kink-like distortion of the tritium β-decay spectrum, caused by the emission of a sterile neutrino, could be located several keV away from the endpoint (see Fig. 1.7). As a consequence, the electron count rate is increased up to levels of 10^8cps, yet the current focal-plane detector is limited to a total rate of 10^5cps integrated over all 148 p-i-n pixels. To handle exceedingly high rate and maintain excellent spectroscopic properties at the same time, an energy resolution of 300 eV FWHM at 20 keV with a multi-pixel silicon drift detector (SDD) and a readout system are currently being developed. The ultimate goal of the TRISTAN detector is to enable KATRIN to reach a sensitivity to the active-to-sterile mixing amplitude at the ppm-level. With TRISTAN system, current laboratory limits could be improved by three orders of magnitude and the parameter space of cosmological interest could possibly be reached [3]. The TRISTAN detectors are being produced at the Semiconductor laboratory of the Max Planck Society (HLL). The read-out (acquisition system) components are developed by the company XGLab, Politechnico di Milano, the institute of data processing and electronics at KIT, and the Max Planck institute of Physics [3].

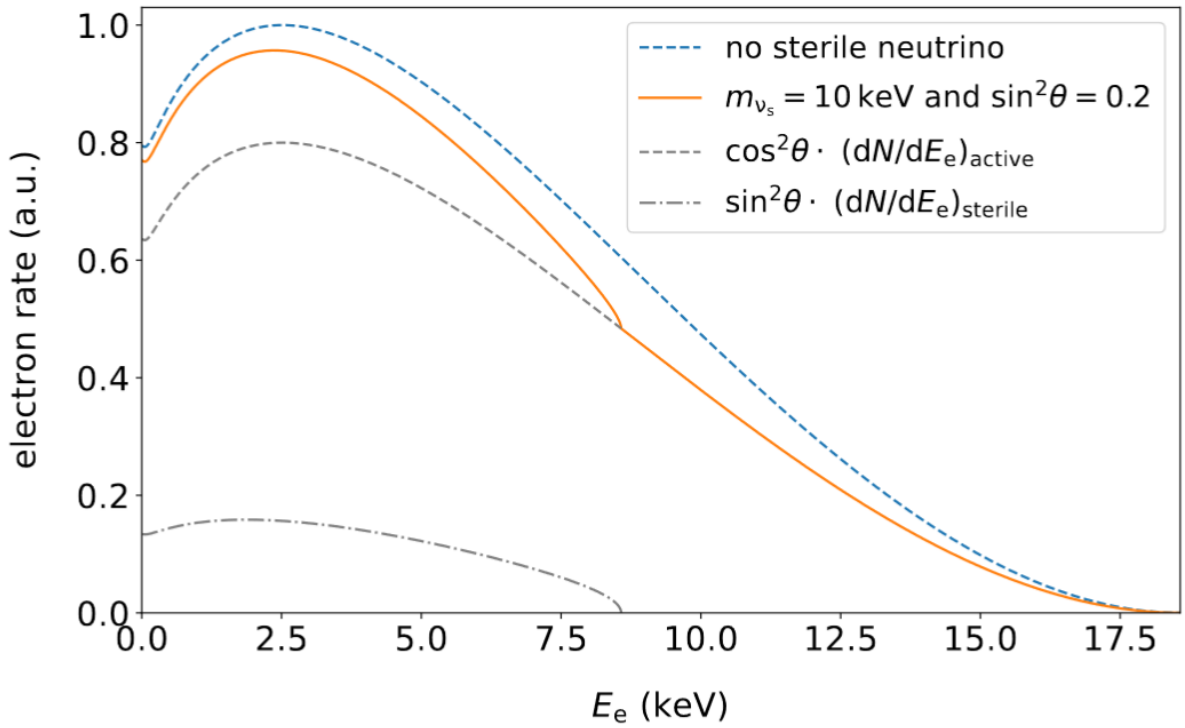


Figure 1.7: Signature of a 10 keV sterile neutrino in a differential tritium beta decay spectrum where: the blue dashed line shows the spectrum without sterile neutrinos. The solid orange line shows the spectrum with a sterile neutrino with $m_s = 10$ keV and an exaggerated mixing amplitude of $\sin^2\theta = 0.2$. The latter is composed of the active branch (gray dashed line) and the sterile branch (gray dot-dashed line) [3].

2 | Acquisition System for the TRISTAN project

In this chapter the different part of the read-out and the SDD detector will be presented to get a general view of the entire acquisition system. There will be a detailed presentation of the SDD technology of and the one developed for the project. The same set of information will be given on the ETTORE board that host the preamplifing ASIC, the bias board that supplies the power and enforces the bias points on the detector. Then there is the Data Acquisition System (DAQ) that filters the signals coming from the SDD, convert them in a digital form and group and displays them for analysis (spectrum extraction,study of different behavior between different pixels, etc...)

I have already mentioned that the KATRIN detector chamber and read-out system will be upgraded to undergo the keV-sterile program with a TRISTAN system after completion of the mass measurement campaign (discussed in Sec. 1.3). "The total number of pixels as well as the size of the final detector must follow these requirements":

- minimizing pile-up events by increasing the number of pixels,
- avoiding charge sharing between adjacent pixel by increasing the size of pixels,
- reduce backscattering by maximizing transverse momentum,
- reducing back reflection into different pixels by reducing Larmor radius,
- keeping a manageable complexity.

All these constraints have been simulated and an optimal configuration was found (in 2016-2017) with 3486 hexagonal pixels of 3 mm diameter. The detector plane will be split into 21 modules disposed as represented in figure 2.2 [10].

2.1. Silicon Drift Detector (SDD)

Low anode capacitance is the key to the superior speed and energy resolution that characterises this technology. Formerly called semiconductor drift chamber, the modern SDD is based on a design by Emilio Gatti [6].

SDDs use the basic principle of sideways depletion, see Figure 2.1.

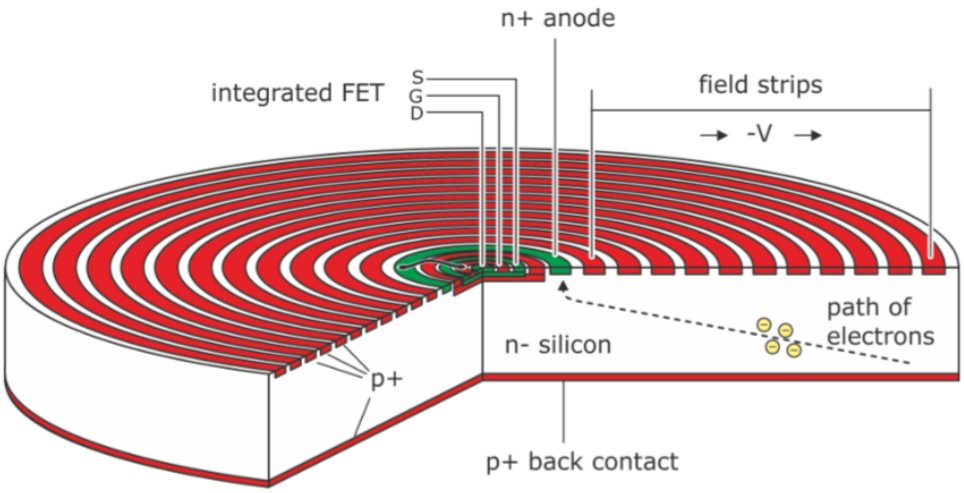


Figure 2.1: Schematic of a single pixel of the TRISTAN silicon drift detector. Electrons are guided by an electric field to the collecting n^+ anode in the center of the detector which is surrounded by several drift rings. The entrance window for radiation is on the opposite side (p^+ back contact). The detector features an integrated field effect transistor (FET) close to the anode which forms the first stage of the readout electronics [3].

A volume of a high-resistivity semiconductor material (low doping concentration), n-type silicon, is covered by rectifying p-doped junctions on both surfaces. A small substrate contact in reverse bias to the p-regions depletes the silicon bulk. The p-junctions are segmented strip-like and biased such that they generate an electric field with a strong component parallel to the surface. Signal electrons released within the depleted volume by the absorption of ionizing radiation drift towards the readout contact, i.e. the collecting anode. Due to the small physical dimensions of the anode, the detector has a small capacitance which is almost independent of the detector area. Compared to a conventional diode of equal area, this feature translates into larger amplitudes of the output signals. The anode of every pixel is read out by a charge-sensitive amplifier (CSA) with a JFET integrated into the anode structure of the chip, followed by a low-noise application-specific integrated circuit (ASIC) specifically developed for the TRISTAN detector. The

integrated JFET allows the ASIC chip to be placed at several cm distance to the detector chip, while keeping the total anode capacitance at only 180 fF. This provides an excellent signal-to-noise ratio. The SDD concept is very flexible in shape and size. However, a large single-pixel detector would have inherent limitations in terms of drift time and count rate. Therefore, the TRISTAN detector system will be based on multi-cell SDDs combining a large sensitive area with the energy resolution and the count rate capability of a single SDD (Fig. 2.2) [3].

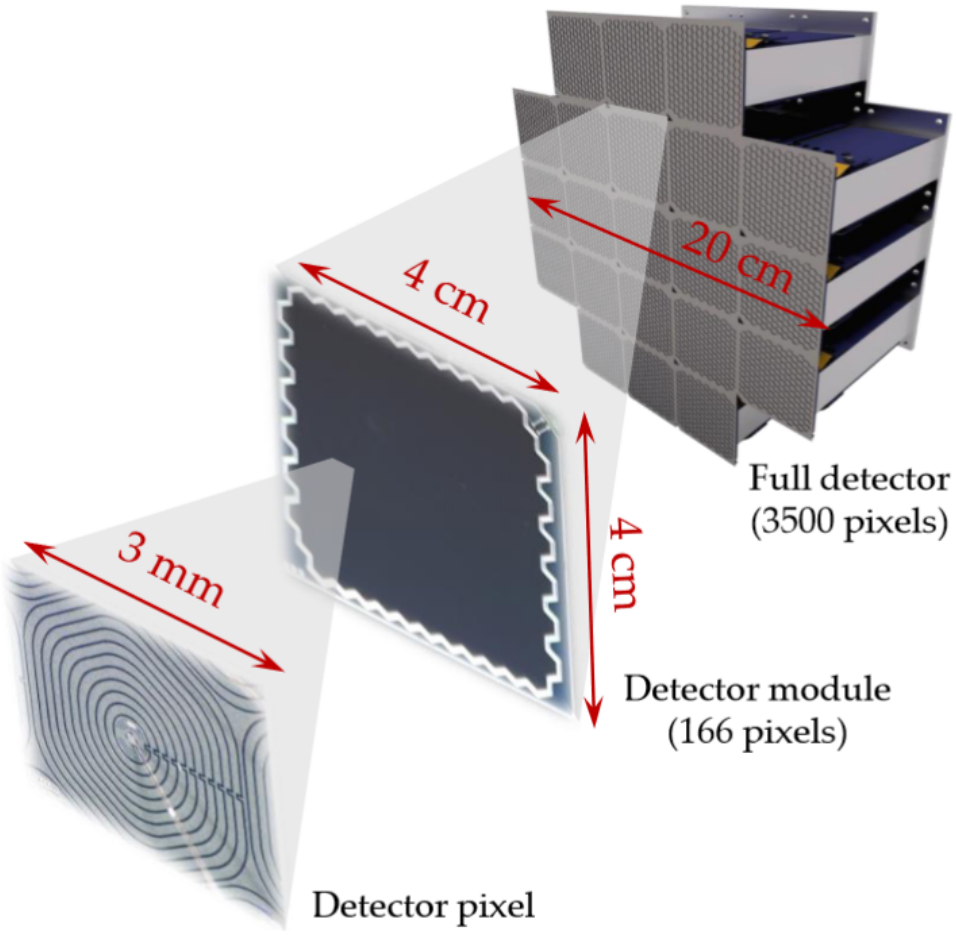


Figure 2.2: Design of the TRISTAN detector. The full detector array consists of 21 identical modules each consisting of 166 pixels. One module has a size of $4 \times 4\ cm^2$ with the individual pixels having a diameter of 3 mm. The pixel anodes are connected to the charge-sensitive amplifier via wire bonds [3].

A multi-cell SDD is a continuous, gap-less arrangement of a number of SDDs with individual readout, but with common voltage supply, entrance window and guard ring structure. The novel detector system is optimized to minimize effects which can alter the shape of the

detector response. The pixel size is chosen to be 3 mm in order to minimize charge-sharing and pixel changes after backscattering and back-reflection. The entrance window has a minimal thickness of about 50 nm in order to minimize energy loss. Detector and readout electronics are optimized for low noise, and thus for good energy resolution. Finally, a full waveform digitization is chosen to minimize the effect of ADC non-linearities. The development of the TRISTAN detector system follows a staged approach. Starting with 1 and then 7-pixel detector prototypes with a simple mechanical design (first without an integrated JFET into the anode structure of the SDD), the detector chip was scaled to a more complex module consisting of 12 and then 47 pixels, which has already been tested successfully. The final focal-plane array will consist of 9 (**phase 1**) and 21 (**phase 2**) detector modules of 166 pixels each [3].

THE NEXT SUBSECTIONS WILL PRESENT THE EVOLUTION OF THE TRISTAN PROJECT IN TERMS OF SDD CHIP CHANGES BEFORE COMING TO THE FINAL 166 PIXEL ULTIMATE VERSION

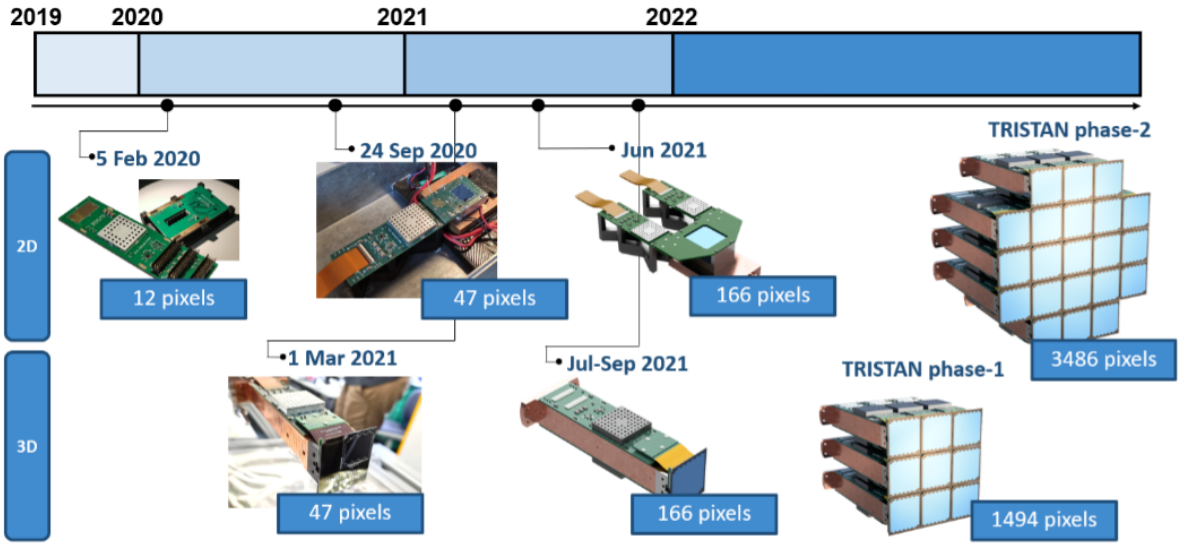


Figure 2.3: TRISTAN project roadmap from 2019 and future phases[11]. *Before and during 2019, there was the characterisation of the 1 pixel SDD with electrons (objective: obtaining empirical information of the SDD response with electrons at energies of the order of tens of KeV). Then the 7 pixel module was produced to verify the scalability of multi-SDDs integrated on the same chip. Going forward, the multi-SDDs technology scales up to 12, 47, and finally to 166 objectives, with different developed versions*

2.1.1. 1 pixel SDD characterisation with electrons

In this section it will be demonstrated that the detector response to electrons is much different and more complex than the response to X-ray photons. The problem with electrons energy detection is the incomplete charge collection occurring in the partially sensitive entrance window region of the detector and the fact that electrons can backscatter. In order to benefit from the high-resolution and high-rate capabilities of the SDDs to measure an unknown electron spectrum, e.g. a β-decay spectrum, a deep study and modelling of the single pixel SDD has been done by Matteo Gugiatti. For electrons, entrance windows effects are always observed, regardless of their energy. This is due to the continuos interaction with the atoms on their path. In literature, only a few articles not related to TRISTAN address the response of SDDs and other Si-based detectors to electrons. A systematic study of the SDD aiming at building a model of the detector response to electrons, is still missing. A methodical characterisation of a single-pixel SDD, has been performed in 2019 employing an electron scanning microscope (SEM) as a collimated and mono-energetic source of electrons (find the characterisation details in: [8]). The SEM is located in the Department of Material Science in University of Milano-Bicocca. The experimental setup is illustrated in Figure 2.4.
The measurements have been conducted with fixed energy settings of 10 and 20 keV. In this energy range, the electronic noise, the incomplete charge collection (due to dead layer effects in the entrance window), and backscattering have a strong influence on the observed energy response. The experimental data acquired a span of results, from the optimisation of the biasing voltages of the detector to maximise its efficiency, to high-statistics measurements of mono-energetic electrons with various incidence angles. This experimental investigation was the starting point to build and validate, through Monte Carlo simulations, the precise physics model of the detector. This model will faithfully reconstruct an unknown β-decay spectrum, starting from its experimentally measured data [8].

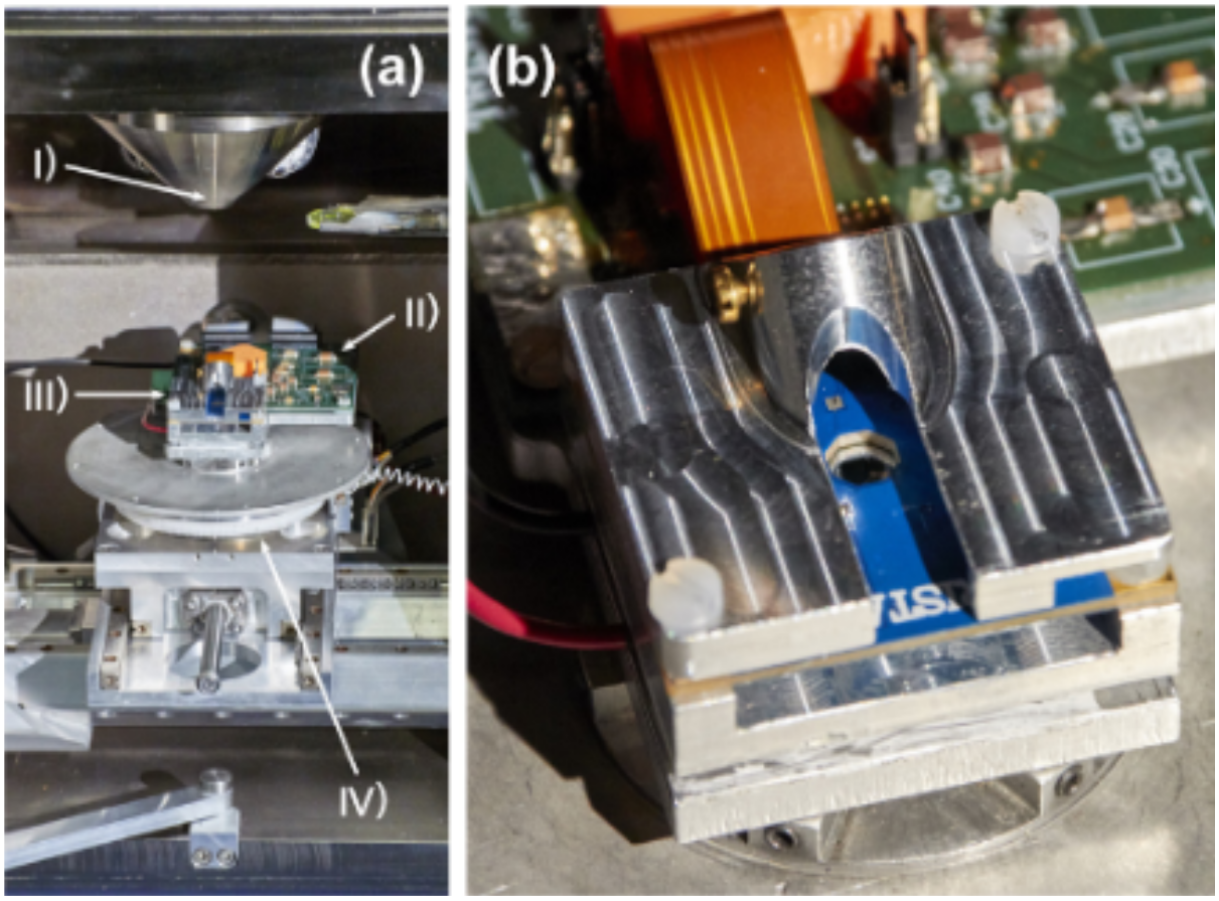


Figure 2.4: Experimental setup installed in the SEM: (I) electron beam source, (II) board hosting the ASIC charge preamplifier and the filter capacitors, (III) detection module with the single SDD, (IV) movable sample holder. (b) Close up view of the board hosting the SDD, seen from the entrance window side, and the aluminium cover to protect the detector and to host from $^{5}5Fe$ calibration source. [8].

The different nature of photons and electrons determines the characteristic energy response to these particles, observed by the SDD. Fig. 2.5 illustrates the absorption mechanism for the two types of particles.
The absorption of a photon generates a photoelectron (photoelectric absorption is dominant at tens of KeV) of equal energy which, for 5.9 keV photons, is statistically well inside in the detector's active volume (for very-low-energy photons the absorption occurs very close to the entrance windows instead). The spectrum originating from a typical X-ray line, neglecting the charge losses during the collection of the photoelectrons, can be considered a Gaussian function.

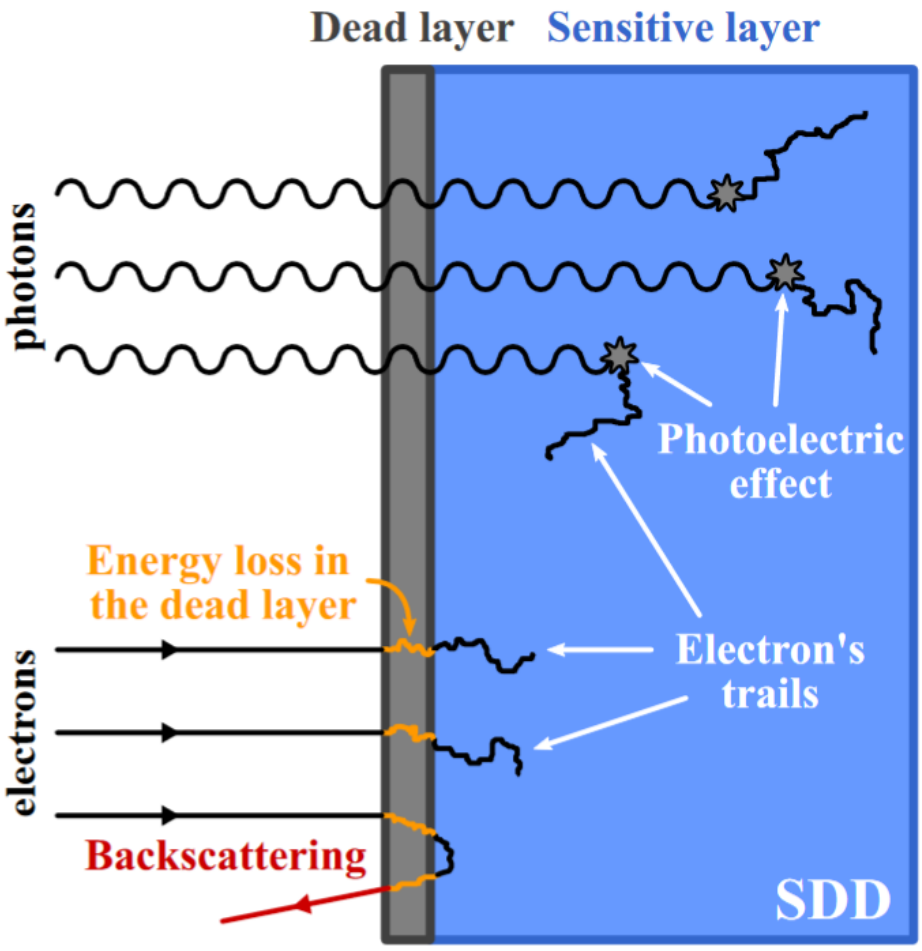


Figure 2.5: Qualitative comparison between the absorption of photons and electrons in a Si detector. The photons in the X-ray energy range are absorbed mainly via the photoelectric effect in Si, generating electron-hole pairs well inside the sensitive volume of the device. In comparison, electrons are absorbed in the proximity of the entrance window and are subject to energy loss in the dead layer and backscattering effects [8].

Electrons, instead, have to interact first with the entrance window before releasing their energy into the active volume, where they will, eventually, come at rest. A part of their energy is always released in the superficial layer of the SDD and cannot be measured. Furthermore, there is the possibility to have electrons which release a part of their energy in the active volume, and then backscatter still retaining a considerable fraction of their initial kinetic energy. The effect of the dead layer and backscattering lead to different features in the response. The dead layer determines the shift, to lower energies, and the asymmetry of the electron peak. Whereas, the backscattering creates a low-energy continuum in the spectrum. The energy resolution obtained with the setup, at room

temperature, was 190 eV FWHM at the $^{55}FeK_{\alpha}$line (5.9 keV) and 265 eV FWHM at the 20-keV e^- peak (calculated by fitting the right-hand side of the e^- emi-Gaussian peak) [8]. The biasing voltages of the SDD shape the electric field inside the detector. The best set of voltages is the one which maximises both the absorption capabilities and the collection of charge carriers generated by the incoming radiation. Two fundamental bias voltages to be optimised are: the V_{BC} (back contact) and the V_{RX} (last ring) voltages which control the depletion of the detector's volume. A series of measurements where each bias voltage is changed step by step and the peak position of a reference incoming radiation is monitored would give the voltage range that yields to the highest centroid position is the good operating region where the electric field optimally collects the generated electron–hole pair. The three-dimensional plot in Fig. 2.6 reports a series of spectra taken at different V_{BC} voltages. A green region can be the best operating condition for the V_{BC} voltage of this 1 pixel SDD [8].

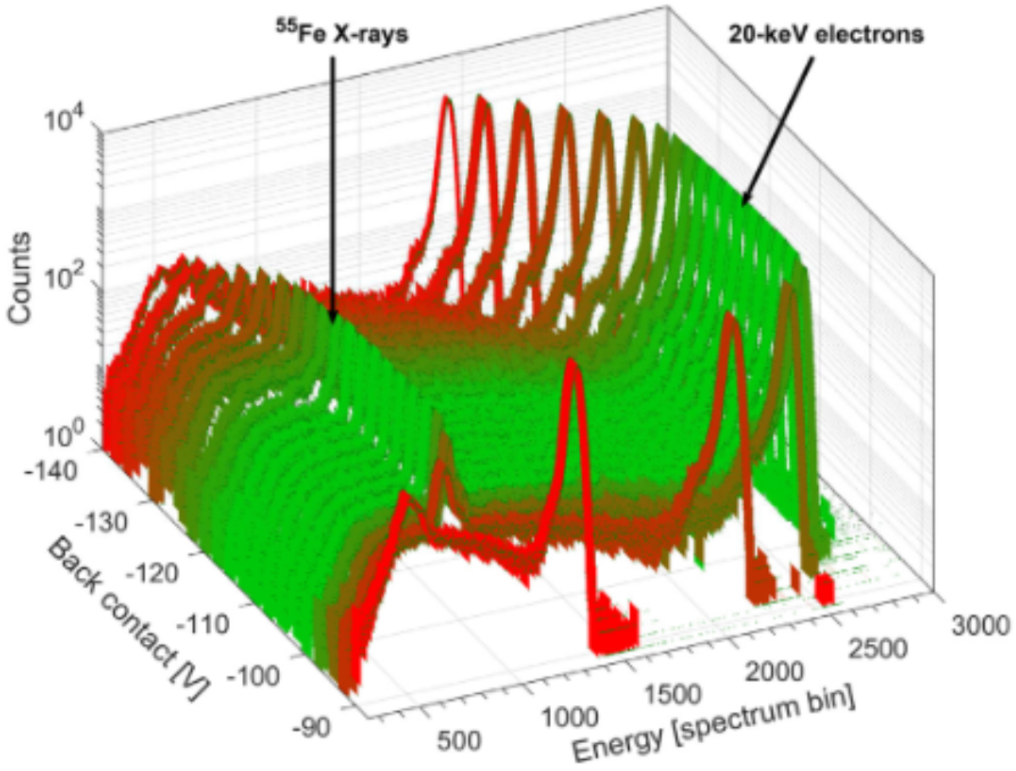


Figure 2.6: Series of experimental spectra with different V_{BC} biasing conditions. The V_{BC} is varied from -90 V to -140 V by 5 V steps. The V_{RX} contact is at -125 V while the V_{BF} contact is always 10 V more negative than the V_{BC} voltage. "The colour of each spectrum represents the position (in bins) of the 20-keV electron peak, green is the full energy" [8].

The availability of a beam with excellent collimation and precise positioning, both in the sub-μm range, allows to study the position-dependence of the detector response. The SDD has been scanned across its 3.2-mm diameter, with a 20-keV e^- beam using 100 μm steps (50 μm steps for the central points). Given the circular shape of the detector, a scan along a single diameter was performed assuming perfect radial symmetry of the device. From the measurements, which are reported in Fig. 2.7, the presence of an insensitive central region of the SDD is clearly visible. The position of the e^- peak, in the spectrum, is rapidly decreasing and disappearing getting closer to the centre of the entrance window. The number of counts drops to zero accordingly. This behaviour is expected for the SDD used in this measurements, where the charge carriers generated above the anode region are collected by the Drain (the most positive electrode) instead of the anode. From the measurements, the dead spot is a circle with a diameter <200 μm which is less than 0.5% of the entrance window's total area, negligible impact [8].

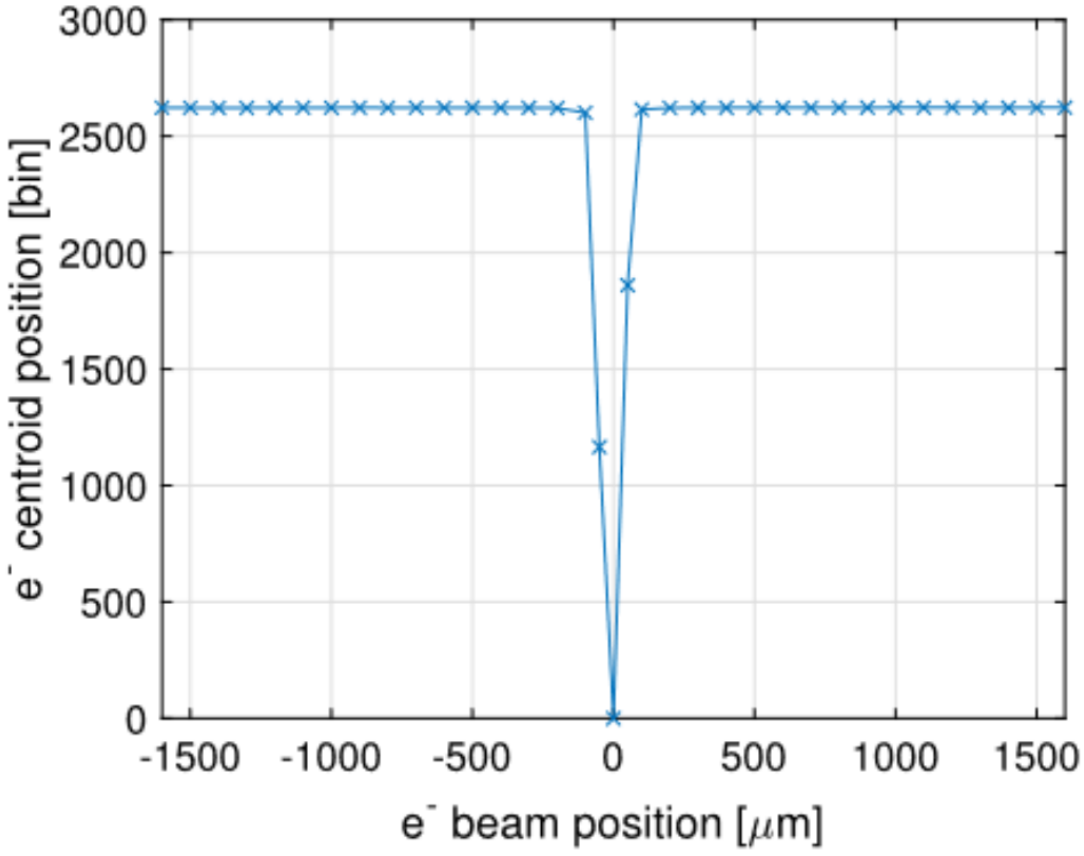


Figure 2.7: Centroid position of the e^- peak versus the position of the beam in different points along the diameter of the SDD [8].

Other studies on the SDD were pursuit to understand:
(the following information are extracted from [8])

- The rise-time performance of the detector.
- The setup, mounted on the microscope's sample holder, can be tilted with respect to the e^- beam. The angle can range from zero, when the beam is perpendicular to the entrance window, up to 65° without losing the line of sight. The amount of energy lost in the passivation layer of the detector, which does not generate any signal, depends on the thickness of the passivation layer itself. If the detector is not perpendicular to the electron beam and it is assumed that electrons travel, in average, in a straight line, the effective insensitive layer that they encounter is increasing with the incidence angle as well as the backscattering effect

2.1.2. 7 pixel SDD

A 7-pixel detector in a planar electronics board configuration was used for X-ray charge sharing measurements Figure 2.8 [18].

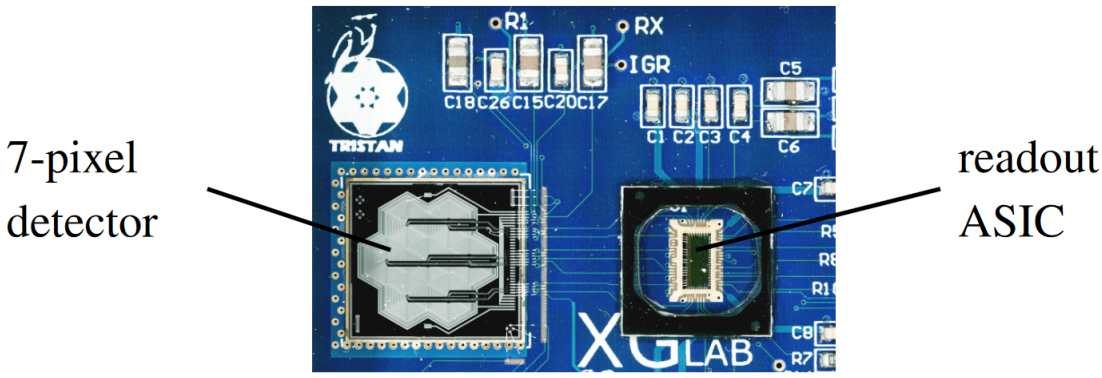


Figure 2.8: Picture of the 7-pixel Tristan SDD detector on its ASIC board [18].

Characterization of charge sharing with 7-pixel SDD

Due to the arrangement of the pixels the charge cloud of an event at the pixel edge will be split between two adjacent pixels. If each pixel is read out independently, this sharing event adds a low-energy tail to the detector response, and the other part of the full charge cloud of this event is collected by the neighbouring pixels. To quantify this effect events in a calibration measurement with an ^{55}Fe X-ray source, the detection was done with a 7-pixel TRISTAN detector. Because the central pixel is fully surrounded by six neighboring pixels, the time coincidence with the neighbours can be used to identify charge sharing events (a coincidence was chosen to have a duration of < 200 ns). Fig. 2.9 shows the recorded ^{55}Fe energy spectrum of the central pixel. By removing charge sharing events (tagged with the <200ns coincident event rule), the low-energy tail in the energy spectrum is reduced significantly. About 2.1% of the events in the central pixel show charge sharing. Using the pixel geometry and the observed energy threshold of 1.3 keV to 1.5 keV, this can be related to a Gaussian charge cloud with $\sigma = (11 \pm 1)$ μm [18].

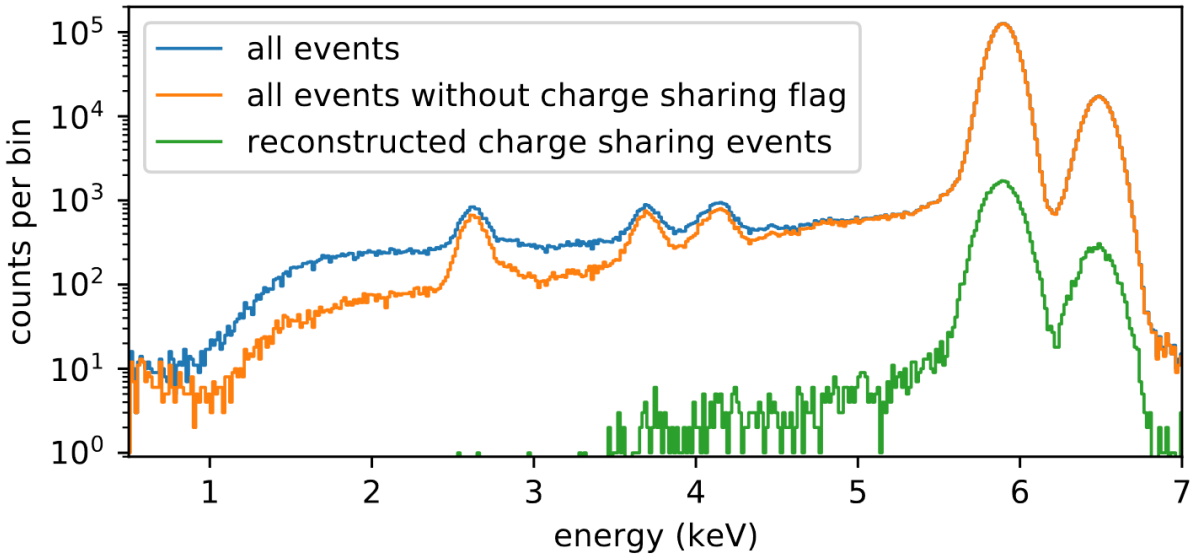


Figure 2.9: Recorded spectrum of the central pixel in the presence of an ^{55}Fe source. the charge sharing chosen by the <200ns coincident event rule contribute to the low-energy tail and can be reconstructed [18].

2.1.3. 12 pixel SDD

12 pixel Detector Board

A representation of the Bonded Detector Board is shown in fig.2.10. The dimensions are 35 mm x 55 mm.

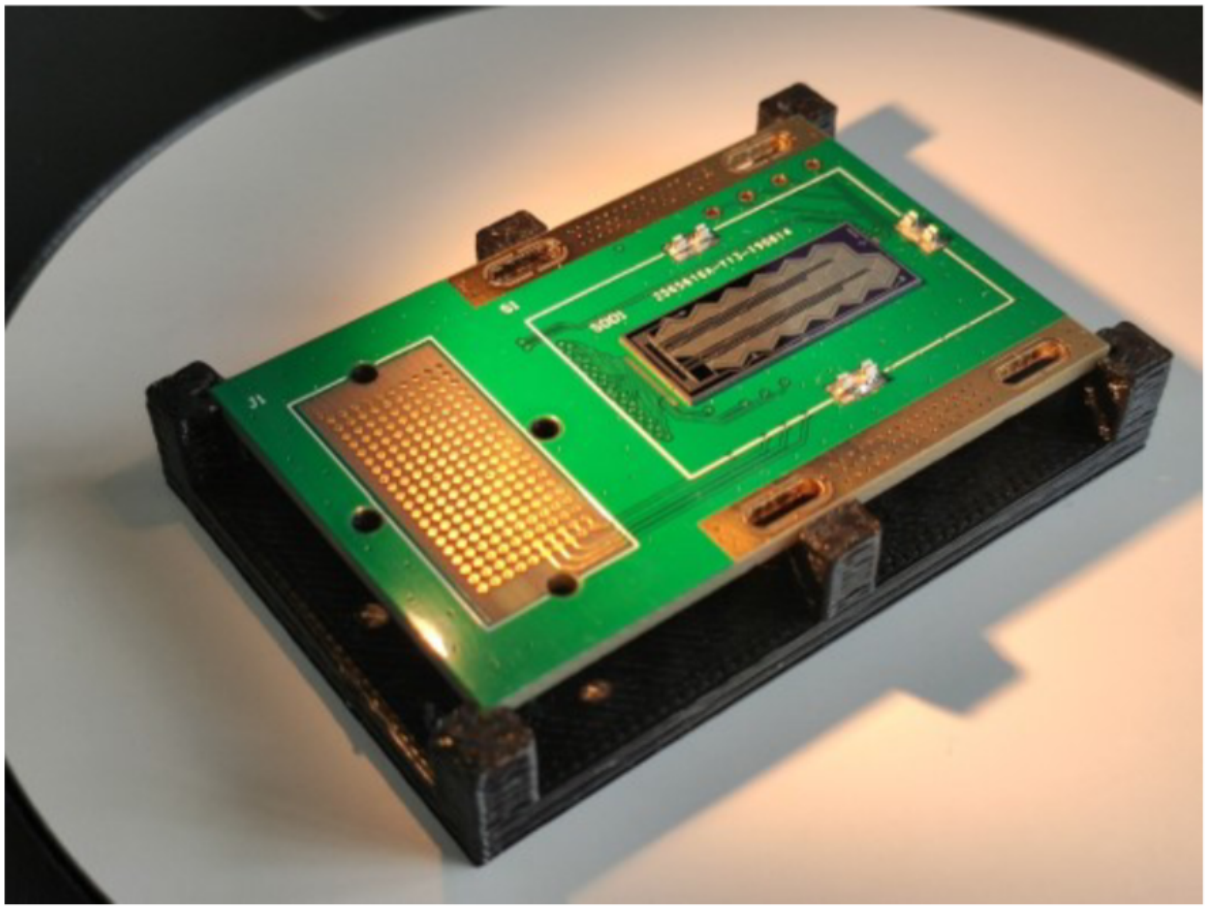


Figure 2.10: The board that host the 12 pixel SDD, that enable the SDD chip to be board to board connected to the ETTORE board (designed for the 12 pixel SDD) [4].

The alignment of the pins requires caution. The bias voltages arriving to the detector board are all filtered using RC networks to avoid additional noises. The pads for each pixel, which are connected to the corresponding channel of ETTORE ASIC, are basically two: IN and CF. They are the source contact of the integrated JFET and the terminal of the feedback capacitor. In Fig. 2.11 there is a simple representation of these connections [4].

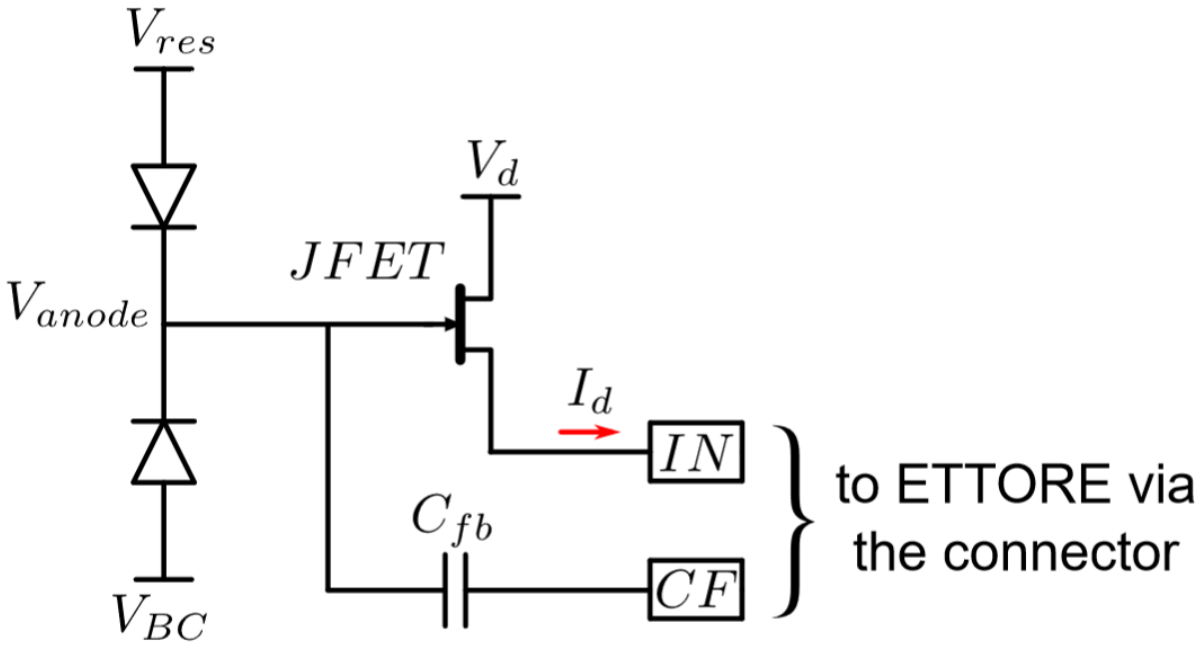


Figure 2.11: The pixel anode and JFet electronic schematic with IN and CF pads for each of the 12 pixels SDD) [4].

The total bondings for this board are 39, 2 on the top side, 37 on the bottom. There are present 24 pads for the **IN** and **CF** contacts for all the 12 channels, along with the connections to the biasing of the JFET and 4 additional ones for a test JFET made with the same technology of the integrated one. There is a hole in the PCB board to allow the X-rays or electrons to reach the entrance window of the SDD. A representation of the physical bonding is in fig.2.12 [4].

Figure 2.12: Picture of a zoomed wire bonding part of the detector board with the 12 pixel SDD[4].

Overview of the 12-pixel setup

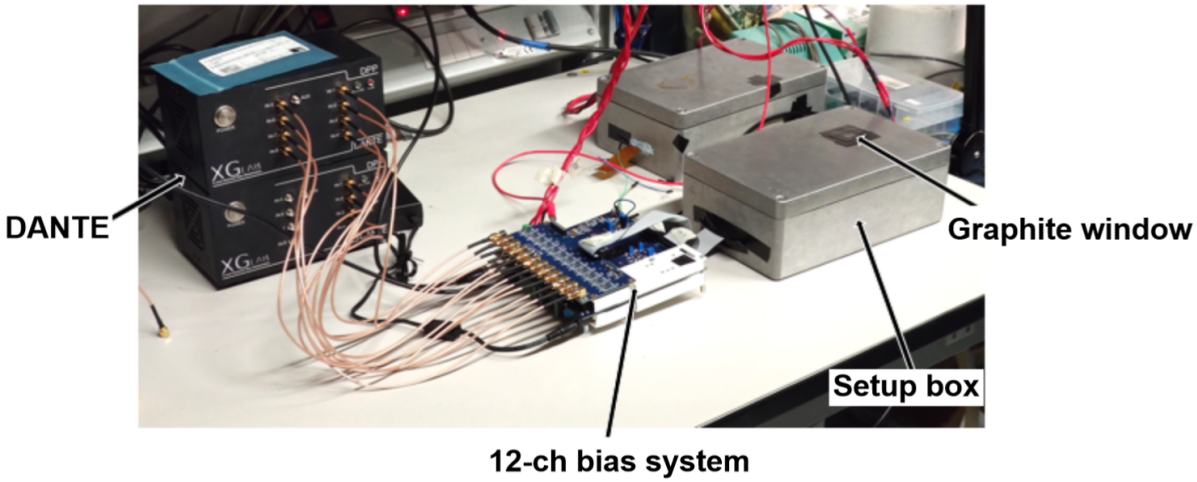


Figure 2.13: Full setup for the 12 pixels detector [4].

Here the 12 pixel setup is presented briefly to have a glance on what is the first evolution step toward the 166 pixel acquisition system Fig. 2.13

- **Detector Board:**
  The detector board is designed to host the SDD Chip. The connection between the chip "pads" and the board pads are made through wire bonding. In Fig. 2.14 you can see the board with the 12 pixels SDD.

- **ETTORE Board:**
  The ASIC board is already structured to be able to connect, with some slight PCB design modification, to the next versions of detectors (47, 166 pixels SDDs).
  e.g. the size of the board is kept as it is from now on and the Samtec PCB to PCB connector is already enough big to be used for the 166 pixel detector [4] (ZA1-20-2-1.00-Z-10 1-mm-pitch 200-pin dual-compression interposer to interconnect the ASIC board and the SDD board).

- **Bias Board:**
  This board is used even for the 47 pixel detector, only with the addition of 2 of the top board which are present on the Main XGlab bias board (at the bottom).
  The board is designed in collaboration with XGLab. Its main functions are to provide the bias voltages and to reset signals to the SDDs and the ETTORE ASICs. The power supply used for this board is a 24 V bench top power supply, and thanks

to its internal DC/DC converters it generates all the voltages needed for the biasing of the detector, HV, BF , BC , V_{SSS} , V_D, IGR, R_1, R_X and the ones needed by the ASICs boards. Moreover, it is possible to make a manual adjustment of these voltages by using the resistive trimmers on the bias board [4].

- **DANTE DPP:**
  The data acquisition system is named DANTE. It is a Digital Pulse Processor (DPP) produced by XGLab. Being the commercial system capable of reading 8 channels, for the following measurements a couple of them were used in a modular fashion. This acquisition system performs a 16-bit sampling and 125 MHz of the incoming waveform and, by means of a trapezoidal shape digital filtering, it allows to acquire the energy spectrum from the detector signals. DANTE is connected to the PC through USB connection: with a dedicated GUI, it is possible to set the filter parameters and acquire spectra or save raw waveform [4].

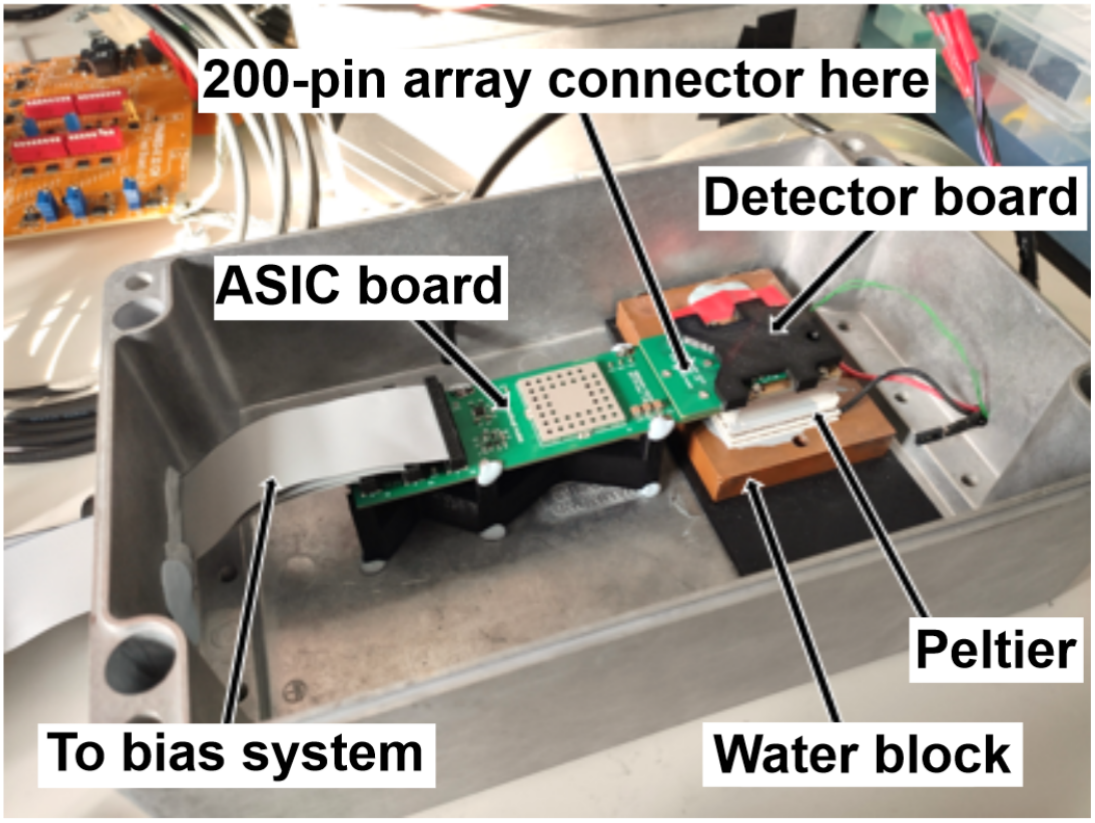


Figure 2.14: Box setup of the 12 pixels detector, the box contains all he ETTORE board connected with the detector to block all the low-energy photon (e.g. visible light is absorbed or reflected almost entirely by the metal box, and humidity is kept under control into a sealed environment) [4].

2.1.4. 47 pixel SDD

This Section present the experimental setup used for the test and characterisation of the 47-pixel planar module. The experimental acquisition system is mentioned to highlight the technology changes required by the new 47 pixels SDD [7].

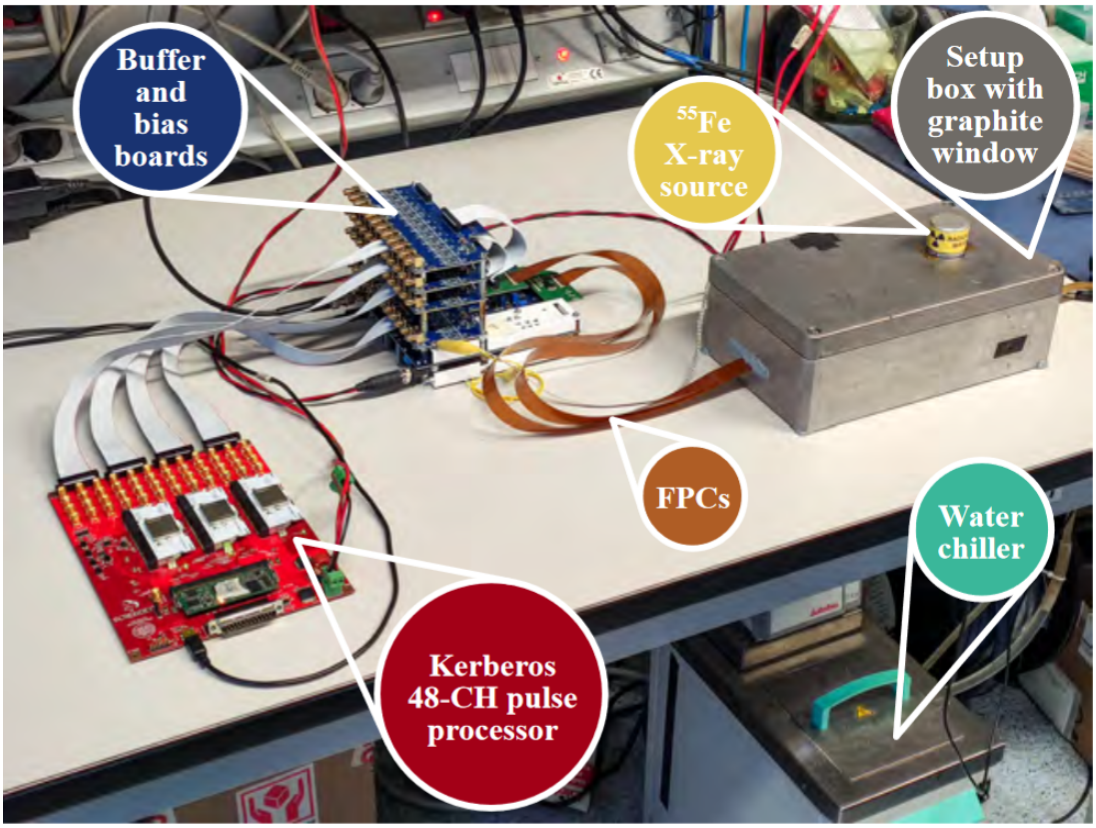


Figure 2.15: Full view of the experimental setup: the setup box containing the detection module, the buffer and bias system and the Kerberos Analog pulse processor [7].

Fig. 2.15 shows the complete laboratory setup of the TRISTAN 47-pixel planar prototype. The detector assembly and the pre-amplifiers are enclosed in a sealed aluminium box. The sealing is necessary for two reasons: shield the very sensitive SDD from ambient light and protects the environment inside the box from humidity [7].
A water chiller circulates cold water, typically at 5 °C, in a heat exchanger inside the aluminium box to extract the heat produced by the Peltier device that cools the detector. The combination of chiller and Peltier element can cool the detector up to -40 °C. At this temperature, the parallel noise contribution, associated with the thermal leakage shot noise, becomes negligible [7].

An external electronic system designed by XGLab contains buffer and bias boards. This system, which is also called bias system, provides power supply and control signals for the ASIC preamplifiers and programmable bias voltages to the SDD matrix [7].
The DAQ used in the Fig. 2.15 is Kerberos, a 48-channel compact and scalable analog pulse processor (APP) developed in Politecnico di Milano. It is made of three 16-channel analog ASICs called SFERA, which perform the signal shaping using 9th-order semi-Gaussian filters in the analog domain [7].
The interconnections are quite different compared to the previous version used for the 12 pixels SDD: these changes were required to accommodate the larger amount of channel signal needed to reach the DAQ from the ETTORE Board. Between the bias system and the DAQ ribbon cables with 2-mm insulation-displacement contact (IDC) connectors are used. The connections between the detection module and the bias system rely on dual-layer flexible printed circuits (FPC), custom-designed by Matteo Gugiatti (former PhD student working on this project). Each FPC carries 100 lines, both signal and power, in a very compact format [7].

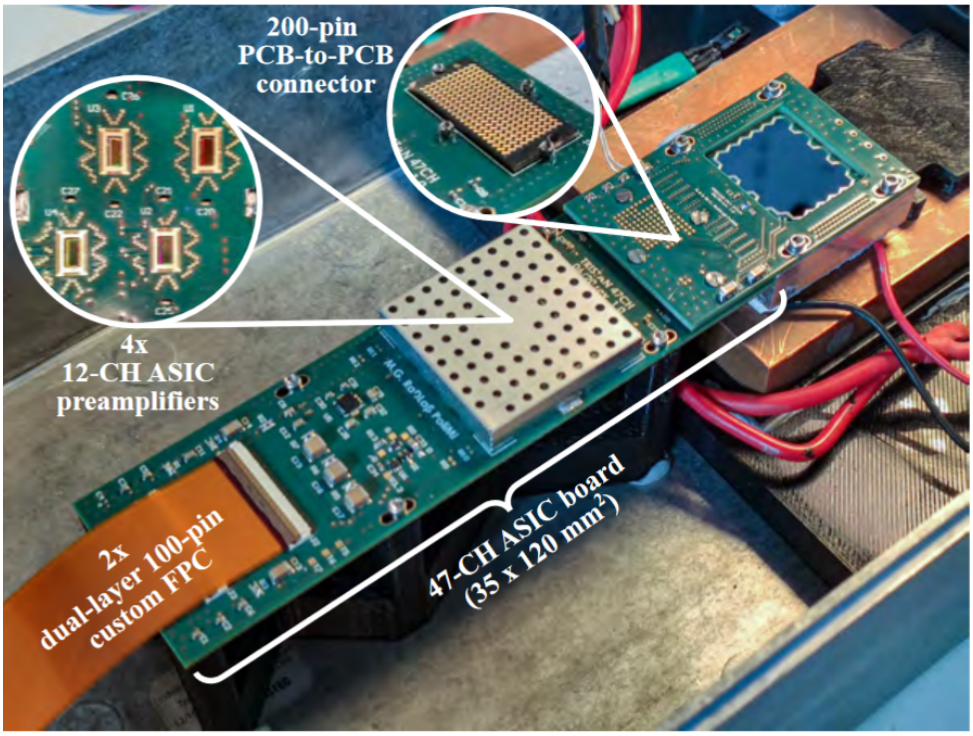


Figure 2.16: Picture of the 47-pixel planar experimental setup contained in the metal box. The ASIC and the SDD boards dominate the view. [7].

Fig. 2.16 shows the interior of the metal setup box where the ASIC board, the SDD board and the cooling apparatus are placed. The ASIC board hosts 4 ETTORE ASICs, power supply filters and a 3.3V voltage regulator for the ASICs' power supply. The connection between the ASIC board and the PCB hosting the silicon detector employs a 200-pin dual-compression PCB-to-PCB solder-less interposer [7]. (The 200-pin board-to-board connection and the pair of 100-pin FPCs are already sized for carrying the signals of the next TRISTAN prototype with 166 pixels.)
Fig. 2.17 shows the monolithic 47-pixel TRISTAN SDD matrix from the entrance window side. The SDD is glued and wire bonded to the detector board.The SDD is glued on its entrance window side along the four edges without touching its active area. The detector PCB is mounted on an aluminium part which is in thermal contact with the cold side of a Peltier cell. The heat generated by the thermoelectric cell is removed by the water heat exchanger [7].

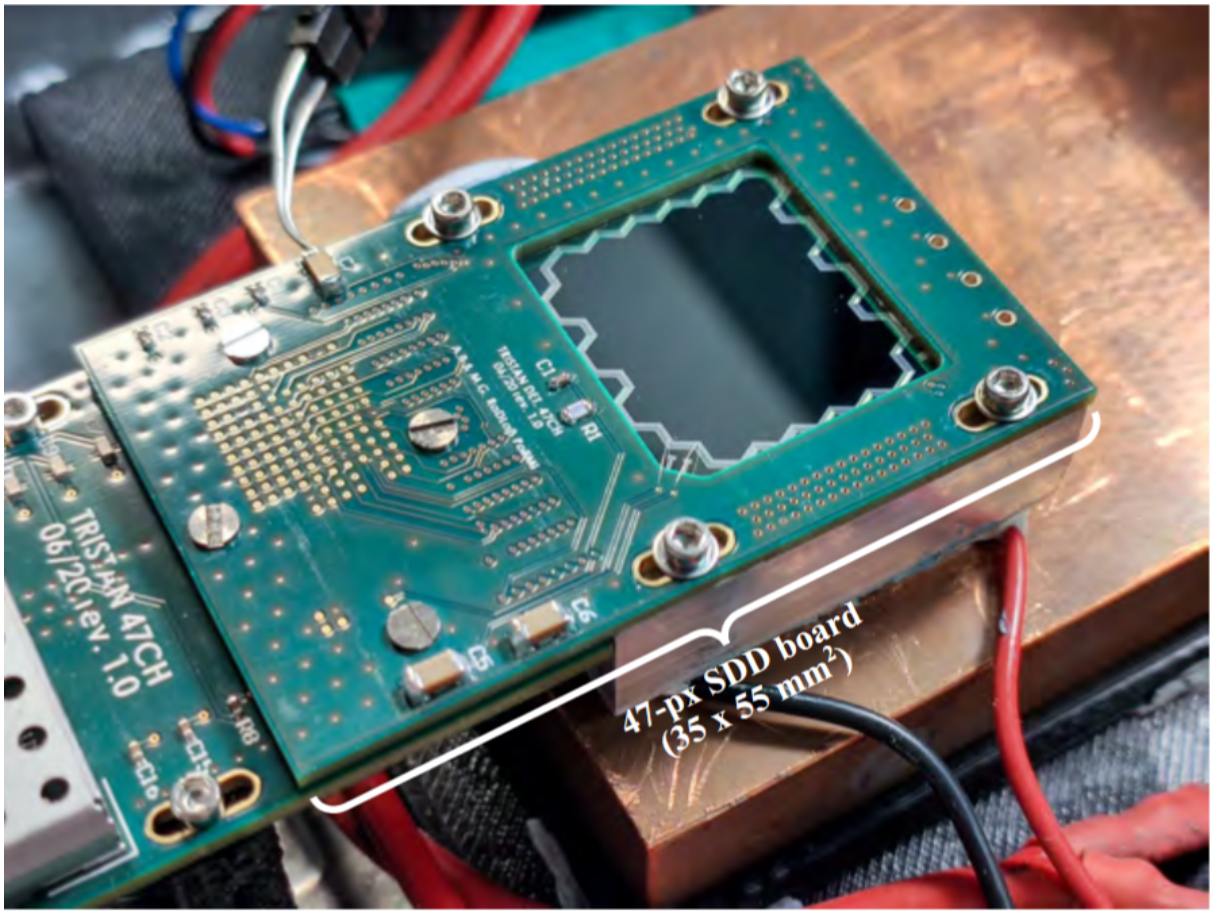


Figure 2.17: Entrance window of the 47-pixel monolithic SDD. The detector is glued and bonded to a PCB supported and cooled by an aluminium structure, coupled to a water-cooled Peltier element. [7].

The 47-pixel Tristan detector module was tested at the monitor spectrometer beamline of the katrin experiment Fig. 2.18.

Therefore the planar setup version presented before (developed at Politecnico di Milano in the RadLab facility) was not the only used to test the 47 pixels SDD.

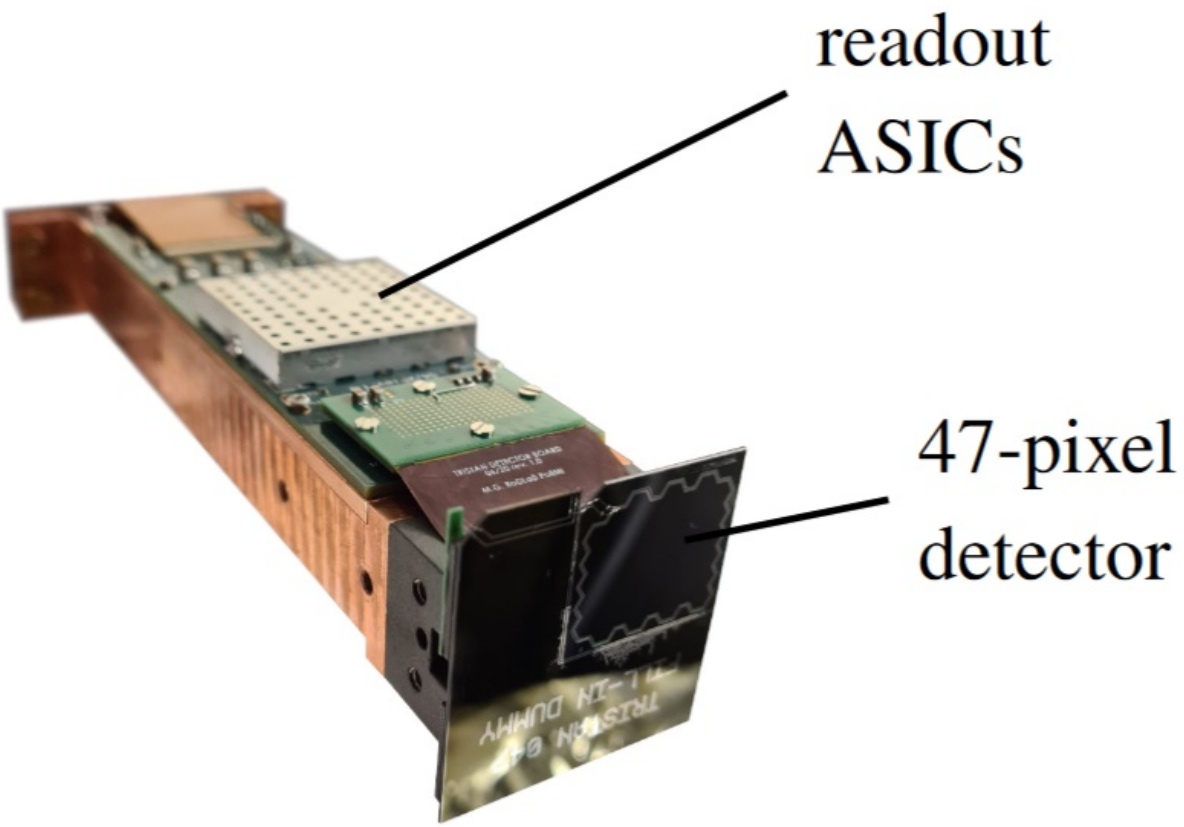
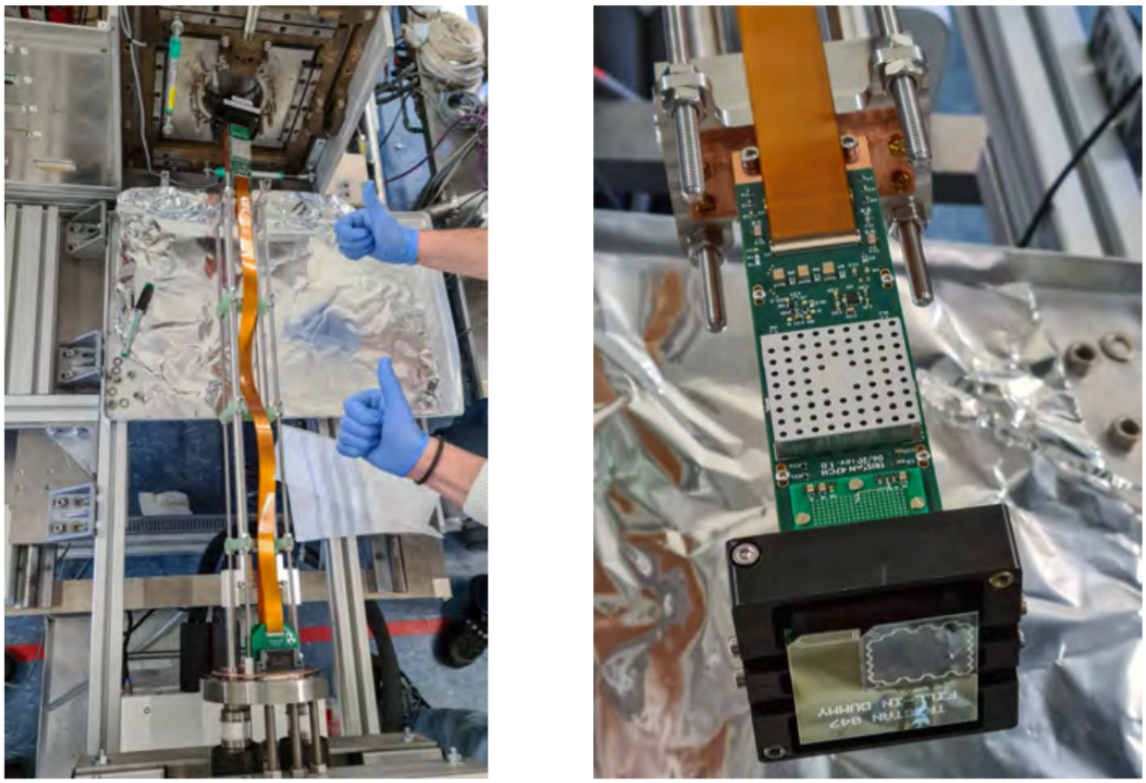


Figure 2.18: 47 pixel 3D module for the test in the TRISTAN beamline. it is well described in this article [18].

another picture of the 47 pixel 3D module for the testing in the Katrin spectrometer:



(a) (b)

Figure 2.19: Pictures of 47 pixel 3D module for the test in the TRISTAN beamline. (a) Suspended cooling and holding structure. (b) Close-up view of the module head with a silicon fill-in part, to make the 47-pixel tile compatible with the CeSiC block designed for the bigger 166-pixel SDD. [7].

Similar to the main beamline of KATRIN, an electron source is combined with a kinetic energy filter (MAC-E filter) followed by the detector. The electron source is a condensed, radioactive ^{83m}Kr source providing several monoenergetic electron lines from internal conversion. The source is set to a negative potential of 1000 V, which adds 1 keV to the kinetic energy of the electrons. In the measurement, the MAC-E filter was set to reject all electrons below the $l_3 - 32$ line (at 31.47) keV, yielding a monoenergetic line from $l_3 - 32$ (conversion at 31.47 keV) and a superposition of l-32 and MN-32 (conversion lines at around 33 keV). The acquired spectra are shown in Fig. 2.20. All pixels show a similar performance and detector response. The rate on the detector varied between 40 cps and 127 cps due to the magnetic field configuration at the beamline. The $l_3 - 32$ line is used to determine the energy resolution which is homogeneously distributed between 320 eV to 360 eV FWHM over the entire detector chip [18].

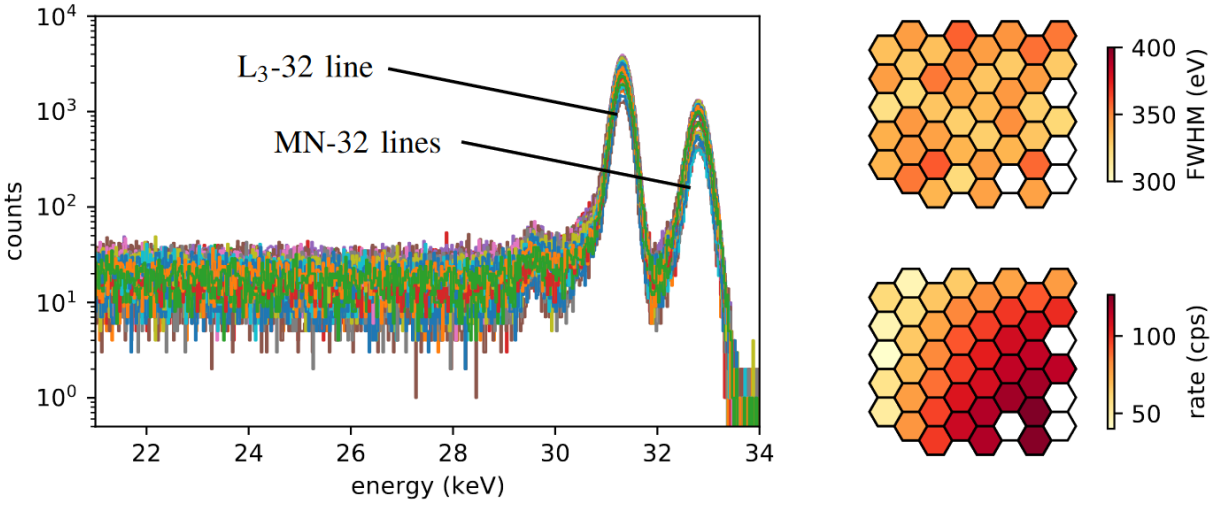


Figure 2.20: Energy spectra of 43 out of the 47 pixels which were read-out at the monitor spectrometer setup. The two peaks correspond to l_3-32 and $MN-32$ conversion electron lines from ^{83m}Kr the pixel maps show the energy resolution (FWHM) and the total rate of the l_3-32 line [18].

2.1.5. 166 pixel SDD

The design and characterisation of the 166-pixel TRISTAN prototype in a laboratory configuration (made in Politecnico di Milano in the RadLab facility) are presented here. The design of the module is an extension of the well-tested and consolidated 47-pixel prototype shown in the previous Sec. 2.1.4 [7].

The main novelty in the 166-pixel design is that two ASIC boards are reading out the monolithic SDD matrix: each one reads one hemisphere of the multi-SDD chip. The 166-pixel detector is divided into two identical hemispheres with 83 cells each (7 reset groups). The signals of each hemisphere (SC and FB lines) are connected to two separate 83-channel ASIC boards. Each ASIC board is equipped with seven ETTORE ASIC, as illustrated in Fig. 2.21 [7].

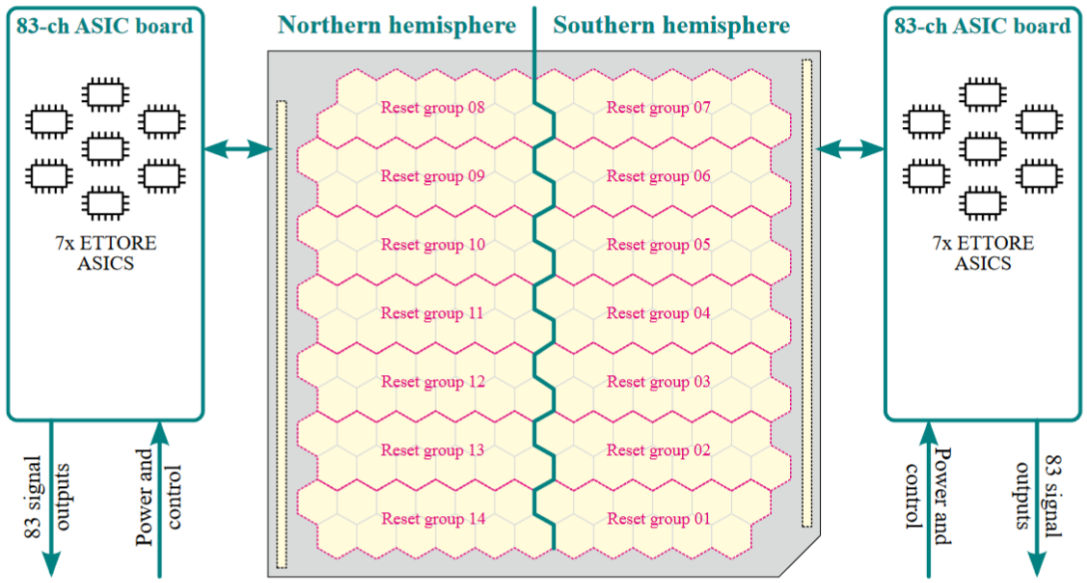


Figure 2.21: Schematic representation of the 166-pixel monolithic SDD readout using two separate ASIC boards for each detector hemisphere. Each ASIC board serves 83 channels and employs seven ETTORE ASICs [7].

166 pixel planar configuration

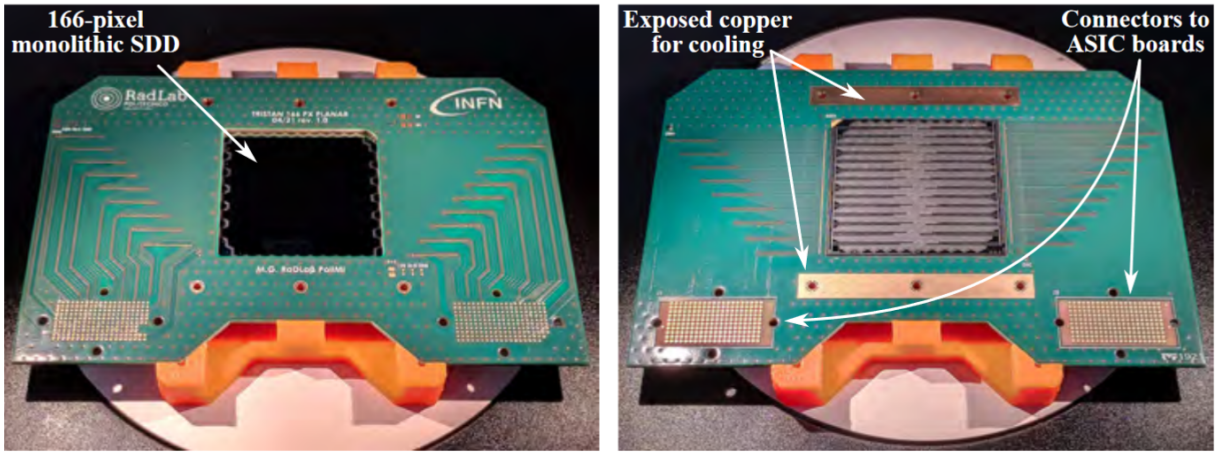


Figure 2.22: Detector board to host the 166-pixel device in the planar configuration. (left) PCB top side with the SDD entrance window (right). PCB bottom side showing the SDD readout side, the 200-pin connectors to the two ASIC boards. The SDD has a total of 361 bond pads that are wedge bonded using a 17-μm AlSi wire. [7].

Similarly to the development of the 47-pixel module, the 166-pixel version has been built and tested in a planar configuration first at Politecnico di Milano. For this purpose, a PCB to host the SDD matrix, as shown in Fig. 2.22, has been developed by Matteo Gugiatti (former PhD student that has worked to develop the ETTORE board, FPC and different evolution of the planar and some 3D testing setup for 1, 7, 12, 47, 166 pixels SDDs). Alternatively, the 166-pixel SDD can be mounted in a 3D configuration using two rigid-flex as done in Fig. 2.27 or Fig. 2.26 for further tests directly on the KATRIN beamline.
The PCB in Fig. 2.22 is designed to connect the SDD bond pads, of both hemispheres, to the two respective 83-channel ASIC boards, via the 200-pin dual-compression PCB-to-PCB Samtec interposers [7].

laboratory planar experimental setup for 166 pixel

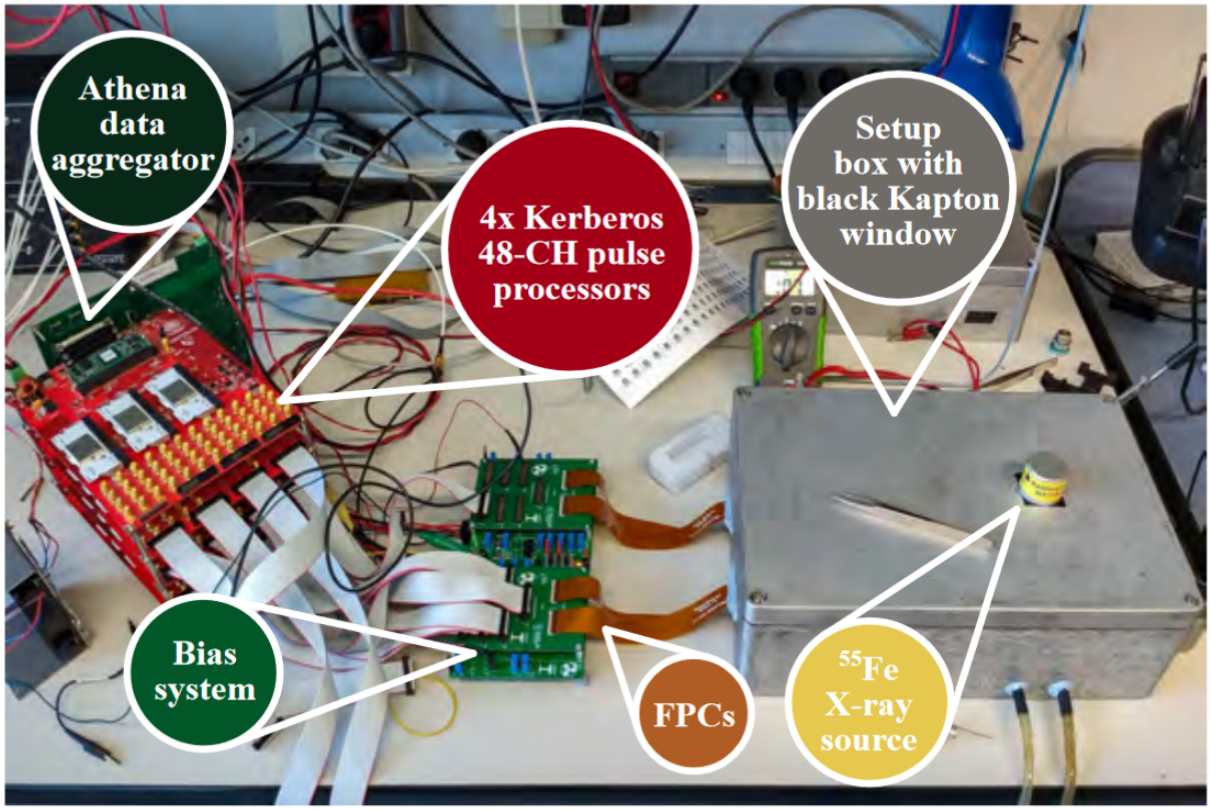


Figure 2.23: Overview of the 166-pixel TRISTAN setup. We can notice the similarity with the 47-pixel planar module. But the 166 pixel one employs a larger box for detector and ASIC boards, a new bias system and a 192-channel pulse processor system called Athena (helped by 4 rows of Kerberos board connected to it) [7].

The experimental setup employed for the laboratory characterisation of the 166-pixel planar module with an ^{55}Fe radioactive source is in Fig. 2.23. The picture illustrates the overview of the experimental setup. The detection module is contained in a sealed aluminium box, that implements the well-consolidated Peltier cell and liquid cooling solution, to refrigerate the SDD detector [7].
The detection module is connected via four 100-pin FPC cables to a custom biasing and control system. The DAQ is a combination of four Kerberos analog pulse processors, that can operate in parallel, to acquire up to 192 channels simultaneously thanks to the Athena data aggregator. The inside of the setup box, containing the 166-pixel SDD and the two 83-channel ASIC boards, is displayed in Fig. 2.24. As usual, the environment inside the box is dry air or nitrogen. The environmental parameters are monitored with temperature and humidity sensors [7].

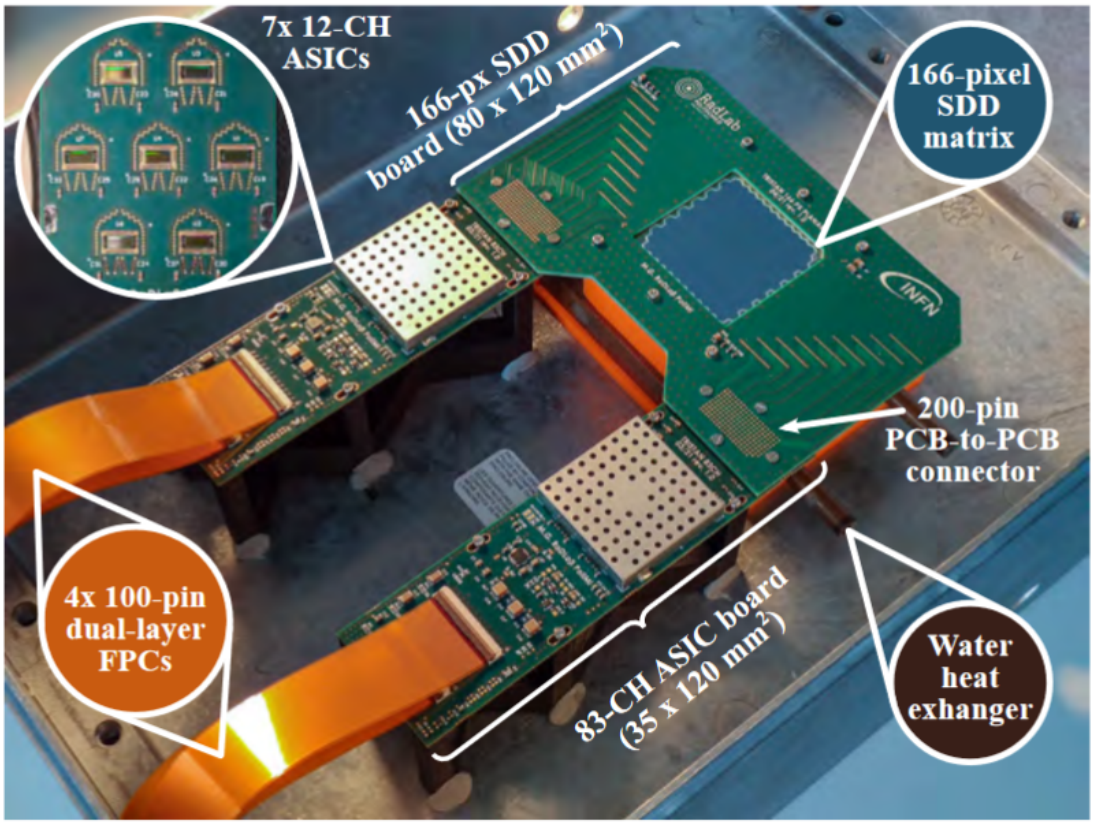


Figure 2.24: View of the aluminium setup box that, when it is closed, prevents humidity and light from reaching the detector. The picture shows the two 83-channel ASIC boards connected to the 166-pixel detector PCB. The detector is cooled by combining a liquid heat exchanger, connected to an external chiller and a Peltier cell [7].

3D prototype for the 166 pixel

Here are presented some images of the 166 pixel 3D module for the testing of the detector in the KATRIN beamline (Fig. 2.25 and 2.26) and the computer design rendering of the single module (Fig. 2.27) for the Phase 1 (9 of the 166 pixel module mounted in parallel in the KATRIN apparatus) and after for the Phase 2 (21 of the 166 pixel module mounted in parallel in the KATRIN apparatus)of the TRISTAN project.

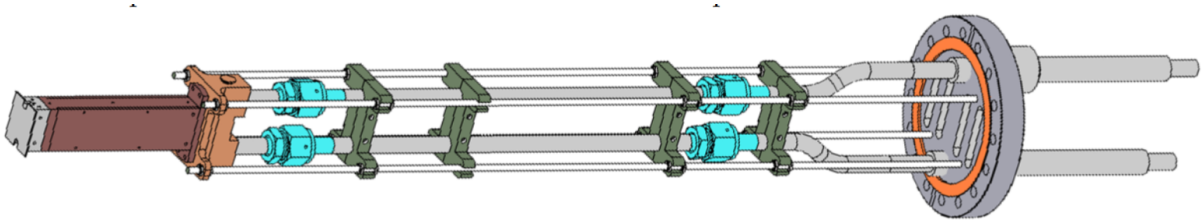


Figure 2.25: First TRISTAN module mechanical setup for single module testing purposes. From left to right: SDD, carbon-fiber reinforced silicon carbide (grey), Copper block (red), heat exchange (orange), cooling pipes (light grey), CF100 flange (dark grey). [10].

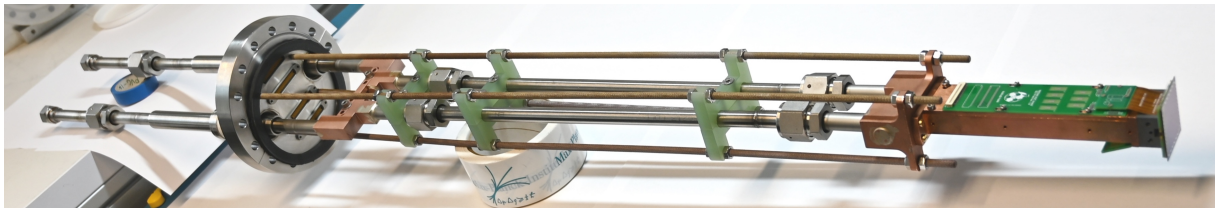


Figure 2.26: First TRISTAN module mechanical set-up. From right to left: SDD, two flexible printed circuits (FPC) connect the SDD and the two opposite sides ETTORE boards in 3D. To complete the picture, when the system will be used for only 1 module testing, a FPC will be present, starting from ETTORE board and going to the Bias board through the CF100 flange (dark grey, in the left-most part of the structure).
Future modules will have different flange structure to be able to have multiple module in parallel for the Phase-1 (9 module) and then for the Phase 2 (21 modules) of the TRISTAN project.
The picture is coming from the MPP lab and was taken in January 2020. The module was used to test its physical structure to verify if everything stayed together and if there were any problems with the insulation for the Ultra-High-Vacuum (UHV) compatibility requirement)

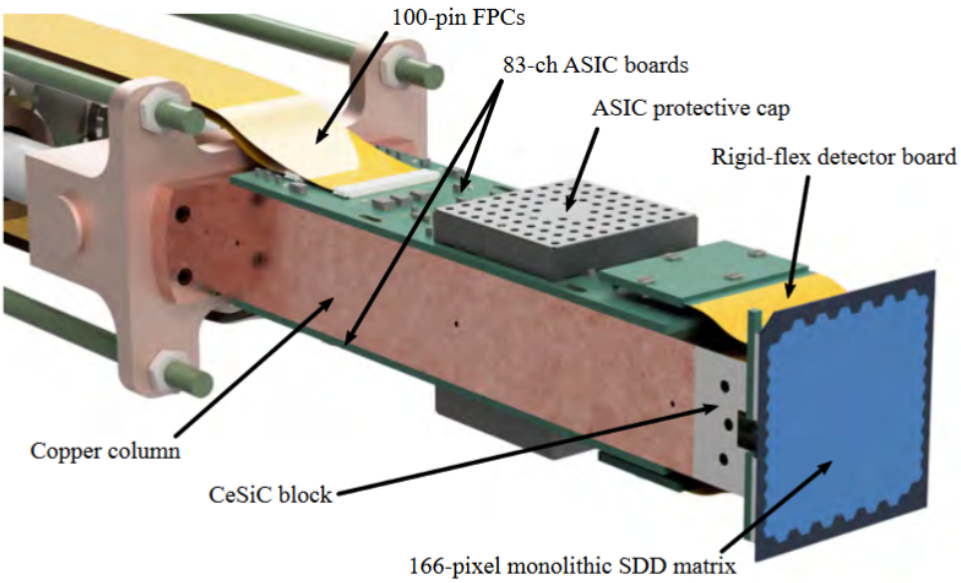


Figure 2.27: Rendering of the TRISTAN 3D module with 166 pixels and its components. The materials are selected to meet outgassing and magnetic field constraints. The same structure has been applied to the 47-pixel module using only one (47-channel) ASIC board and a single rigid-flex detector board in Fig.2.18 [7].

New prototype for the 166 pixel detector

During the first half of 2022 Peter Lechner (of Max Plank Semiconductor Laboratory) has studied solution for a series of problem discovered during the characterisation of the 47 pixel layout done by Korbinian Urban, PhD student at MPP (Fig. 2.28).

- The bond pads were not enough isolated between each others and some coupling effect could occur. To solve the issue, the thickness of the oxide separator was increased, the pads area was reduced and n-implantation was done under the field oxide between the pads
- bBecause of the voltage drop along drain bus line, caused by polySilicon bridges and the inhomogeneous distribution of FET currents (in the 47-cells, 166-cells), the biasing potential on the JFET drain was not enough reliable. As a consequence some bus support structure was introduced
- To solve the cross-talk effect between the signal or bias lines, all the solution described in the first point were applied. The further improvements consisted in making the lines thinner, separating each pixel group of lines and increasing the isolation layer that separates the lines from the SDDs under.

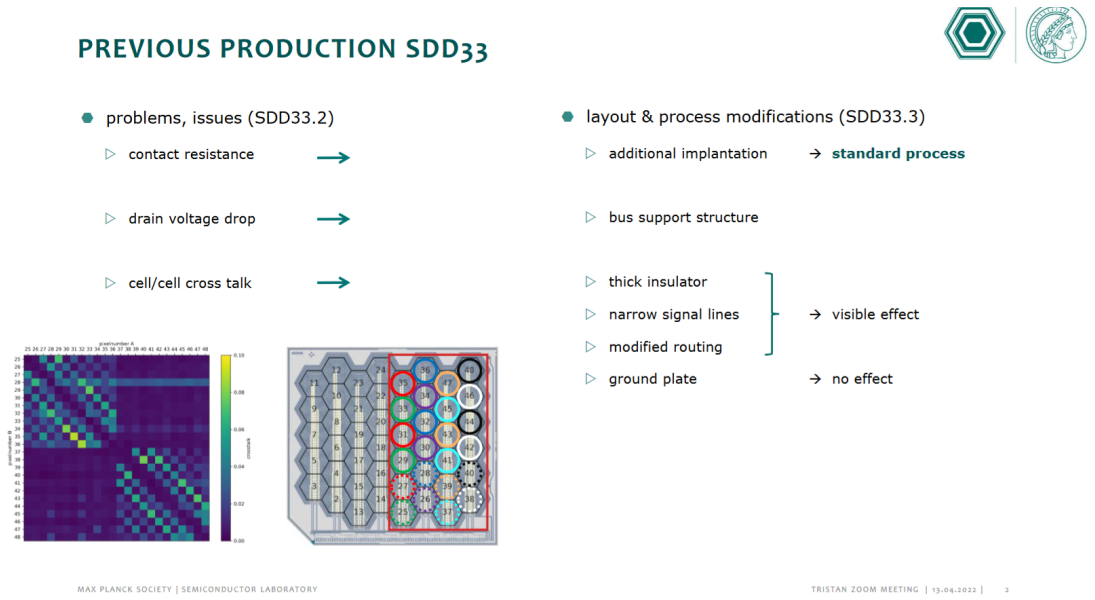
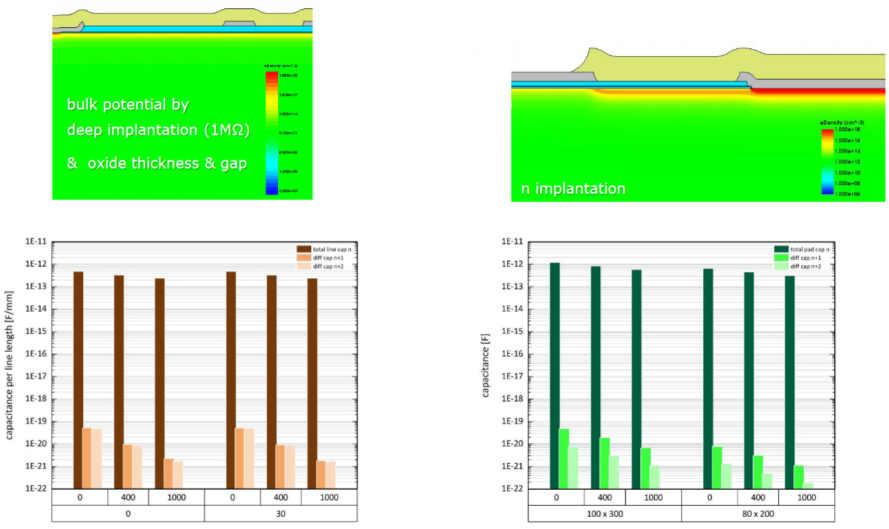


Figure 2.28: The Slide from Peter Lechner's presentation on the problem discovered after testing the 47 pixels.

The simulation result on the coupling decrease between lines and between pads was astonishing. The capacitance coupling values went from $\sim 10^{-12}F$ to $\sim 10^{-19} - 10^{-21}F$. The greater contribution was given by the n-implantation used to better decouple lines and pads (in Fig. 2.29).



(a) CONNECTION LINES SIMULATION.

(b) BOND PADS SIMULATION.

Figure 2.29: The two simulations on the coupling capacitance compared with the values of the former 166 pixels detector design.

2.2. ETTORE (ASIC) board

The ETTORE board first purpose is to pre-amplify the signal coming from the JFETs (each one is on the center of the pixel of its detector) and to send the resulting signal to the DAQ through the bias board. Then, because of its central position in the acquisition chain,it also provides the bias points, coming from the bias board, to the detector.

We have already seen a glance of the development history of the ETTORE board through the evolution of the SDDs (Sec. 2.1) during the Tristan Project time. But a detailed discussion on the topic could bring better insight on how and by what the development of the new ETTORE board prototypes was affected.

2.2.1. The ETTORE ASIC

The ASIC has been named ETTORE after the Italian physicist Ettore Majorana who has contributed significantly to neutrino studies.
This ASIC has been costume designed by XGLab in collaboration with Politecnico di Milano to readout the TRISTAN matrices and **is used throughout all the prototyping phases of the different multi-SDD detector technology produced**. The ASIC will be used until the end of the TRISTAN project (unless some unexpected disruptive project reversal occurs). The design density, arising from TRISTAN's large number of pixels, alongside their small size, well motivates the adoption of an ASIC for the electronics front end. The ASIC is a charge preamplifier for SDDs with integrated JFET and it is realised in the 0.35 μm AMS (name of the company) CMOS technology. Each chip comprises 12 channels to match the "reset groups" on the detector matrices and has an area of $\sim 6.5 mm^2$ (Fig. 2.30). The chip is powered by a single 3.3 V supply and has a power consumption of $21 \frac{mW}{channel}$ [7].

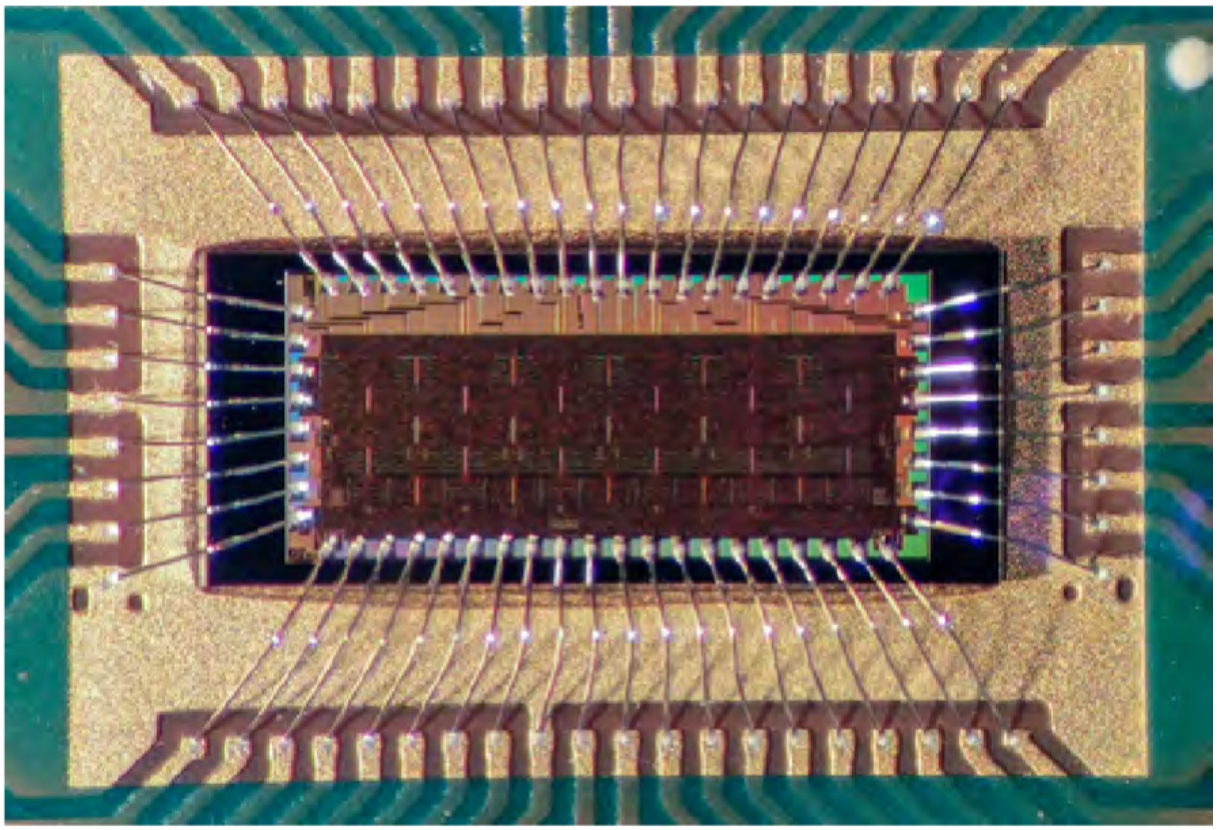


Figure 2.30: The ETTORE ASIC mounted on a TRISTAN prototype PCB. The 56 pads are wedge bonded with a 25 μm AlSi wire. The chip is glued with a thin layer of epoxy to minimise the thermal resistance to the exposed copper plane. The chip measures 3.8 $\times$ 1.7 mm^2. [7].

Each ASIC channel consists of (in Fig. 2.31):

- A preamplifier forming a feedback loop with the n-JFET and feedback capacitor C_{FB}, which are both integrated on the detector chip,
- A comparator to detect the saturation of the output of the CSA,
- A second AC-coupled stage with additional gain and 15 μs exponential decay constant.

To allow for good pile-up rejection, which is required to cope with the experiment's high electron rates (beginning of the Sec. 2.1), an output rise time of less than 50 ns has been targeted as channel performance, even in the presence of stray capacitive loads up to 40 pF, caused by the connections between the detector JFET and the ASIC (SC and FB

signal lines) [7].

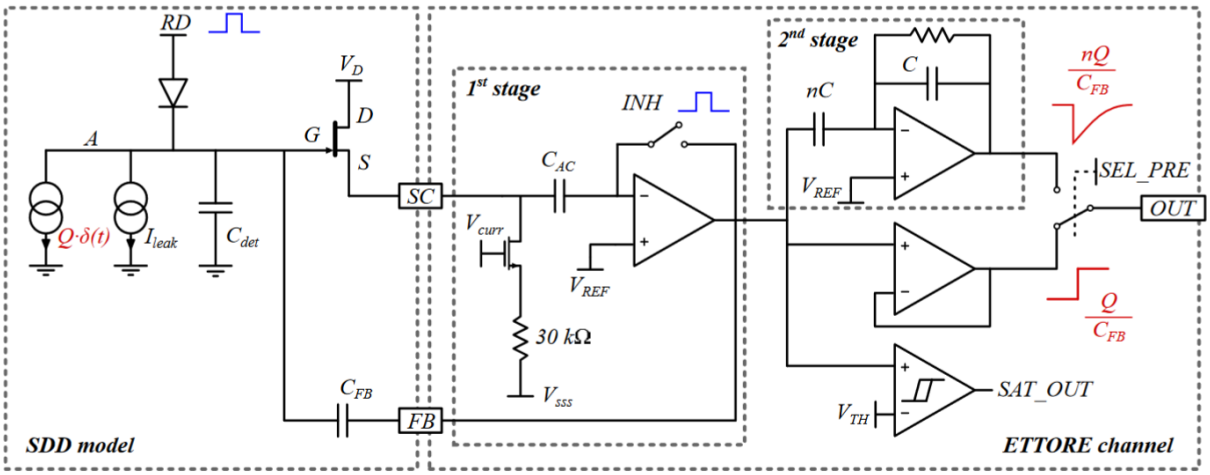


Figure 2.31: Simplified schematic block diagram of one ETTORE channel coupled to an SDD with integrated JFET and feedback capacitor. [7].

The component in Fig.2.31 are described here:

- **The capacitance $C_{AC} = 10$ pF** introduces a low-frequency pole to decouple JFET bias and signal currents

- **Thanks to the V_{curr} and V_{sss} voltages**, it is possible to modify the current generator that sets the JFET bias current (range 50 $\div$ 400 μA)

- **The output of the chip is a 50 Ω line** that can select either the first or second stage output, employing an internal multiplexer, controlled by the SEL_PRE digital signal

- **The buffered first stage output signal**, featuring the classical voltage ramp signal, with superposed steps in correspondence of the events (is meant to be read by a standard digital pulse processor or by an analog shaper)

- **The second stage output signal** requires a deconvolution operation (which might be performed both digitally or analogically) but has the advantage of introducing a gain factor n (equal to 5 or 10), without sacrificing the dynamic range since the

AC-coupling has removed the ramp component.

2.2.2. 12 pixel (first) ETTORE board

The ASIC (or ETTORE) board for the 12 pixels SDD is shown in fig. 2.32, with a dimension of 35 mm x 120 mm. To avoid the accidental damage of the bonding wires during the handling, the ASIC was covered with a special squared metallic case (for the final phases of the TRISTAN project it will be a usefull shield even from the high electromagnetic field experienced in the KATRIN beamline). The voltages necessary for the operation of the ASIC (the power supplies, the static bits and the reset signal) come from the bias board, instead the outputs of the ASIC are sent to it. ETTORE (ASIC) is a chip able to sustain 12 channels at the same time, so with our detector having 12 pixels, all the channels were used. To avoid as much as possible the capacitive coupling (between different signal lines), all the routing of different signals are divided by ground planes, present in every layer of this PCB. A voltage regulator is also present (3.3 V, 600 mA) for the ASIC and a switched reset filter, for the filtering of the reset signal going to the SDD. The former is used to have a more stable supply for the ETTORE board, the latter filters the reset signal, using a capacitor, during the working phase of the detector. *(Note : the reset diode (RD) is a good spot to inject disturb into the signal line of the SDD pixel, so a filtering action is needed. This RD line carries a time-varying signal (reset pulses), and any passive filter would be ineffective. The solution, to avoid disturb and noise contribution on the pixel signal, has been to implement a switch-mode active filter that connects a filtering capacitor to the RD line, only during the CSA charge integration phase, while the RD signal is low and the reset diode is inversely biased. [7])*
The ASIC board, as anticipated, is connected to the detector board through a commercial connector, made by Samtec. It was chosen thanks to its features of compactness, reliability and adequate number of pins. In addition it allowed the swap of different detectors in the setup, since it offered compatibility with older pixels (simply using fewer channels of the ASIC and a different detector board) and the newer one with the 47 and 166, resulting in nearly no additional work on the setup. The connections to the bias system are made through a three 30-pin flat cables, mating exactly to the connectors of the bias board, with a 1:1 correspondence on each signal (this connector is left behind, in the next detector setups, for more advanced connector technology) [4].

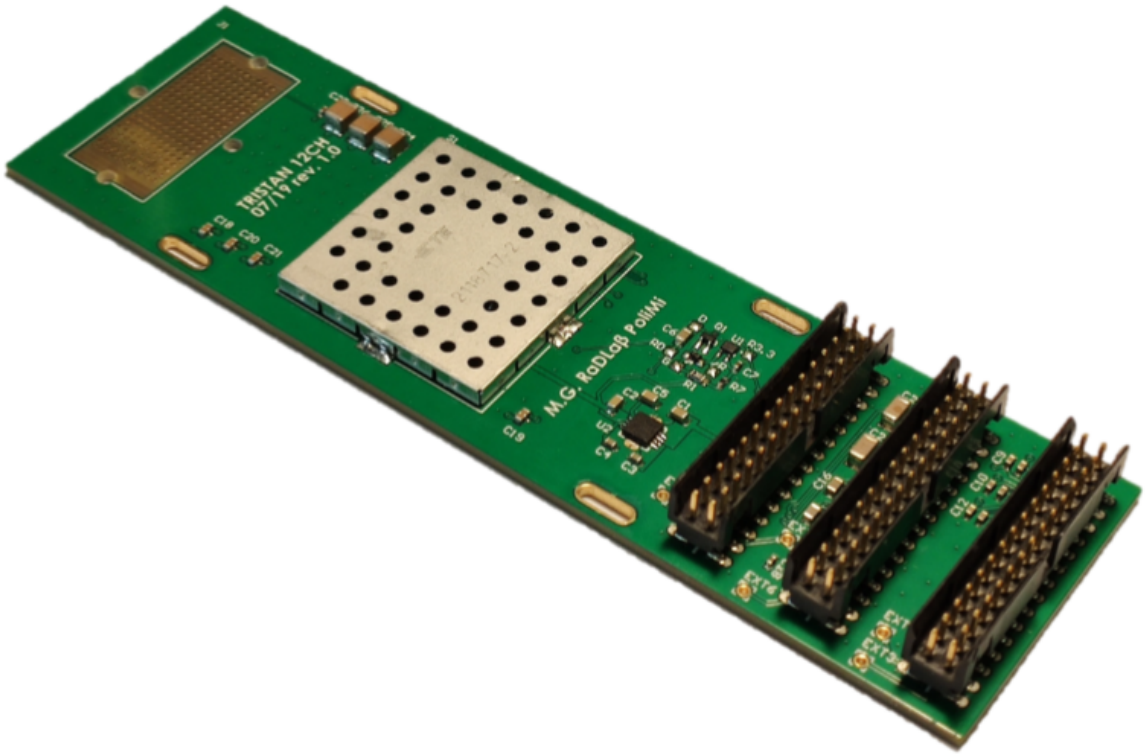


Figure 2.32: The 12 pixels ETTORE board [4].

2.2.3. 47 pixel ETTORE board

The 47-channel ASIC board is a high-density 8-layer PCB that measures 120× 35 mm^2 with standard 1.6 mm thickness. The base material is FR-4 and the surface finish is ENEPIG (electroless nickel electroless palladium immersion gold). The ASIC board design is pretty dense to accommodate the ASICs and the signal tracks in the restricted space dictated by the TRISTAN mechanical requirements. Fig. 2.33 shows a view of the PCB rendered by the CAD software employed for its design. The upper part, in the figure, illustrates the top view of the PCB where all the components and ASICs are allocated. The other side of the PCB is component-free, so it can lay flat on the support and cooling structure. The lower part of Fig. 2.33 shows the PCB internal layout with tracks, pads, and vias [7].

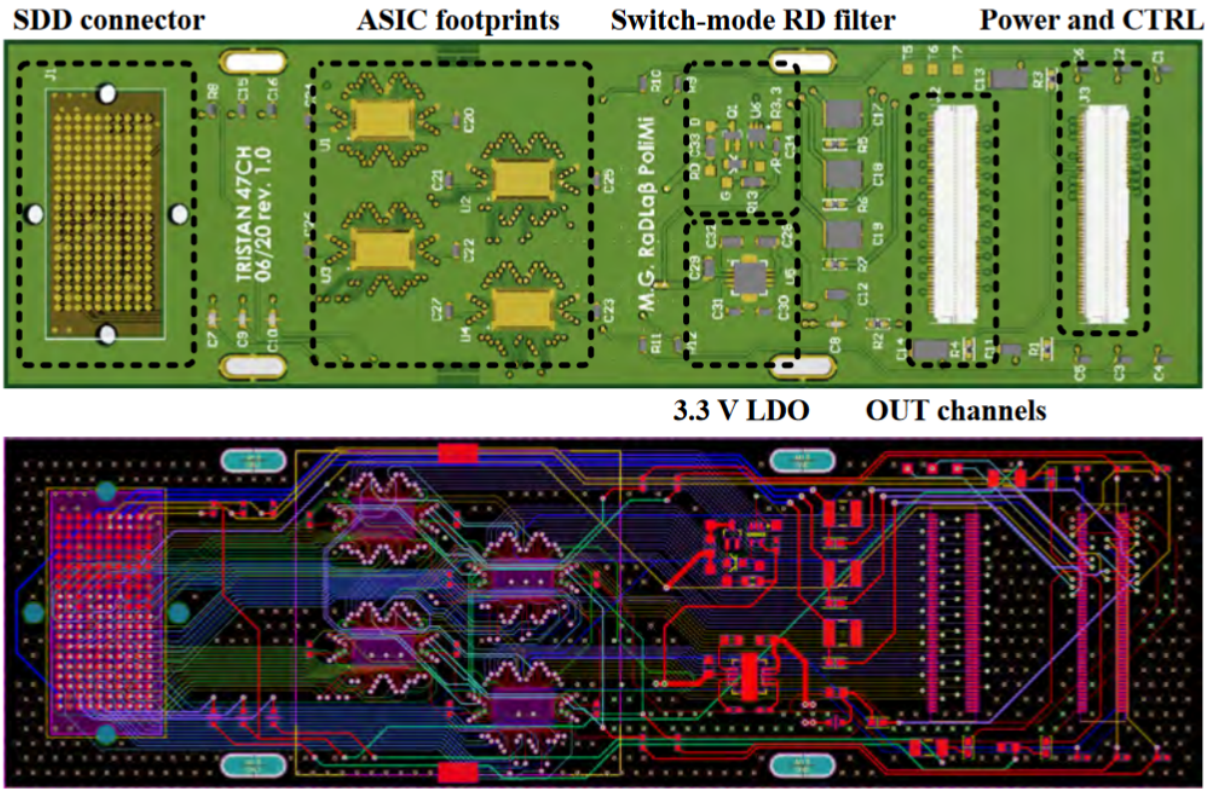


Figure 2.33: the 47 pixels ETTORE board [7].

The main blocks and their function are explained in the following list:

- **SDD connector.** No changes undergo from the 12 pixel ETTORE board, the Samtec ZA1-20-2-1.00-Z-10 1-mm-pitch 200-pin dual-compression interposer to interconnect the ASIC board and the SDD board. It allows the test of multiple SDDs using the same ASIC board just by replacing the interposer regularly [7].

- **ASIC footprints.** apart from the number (now 4) of footprints (where to glue and bond the ETTORE ASIC), no changes undergo from the 12 pixel ETTORE board. The footprints have an exposed copper region below each ASIC to maximise the heat transfer to the PCB layers [7].

- **Switch-mode RD filter.** This is an active filter for the reset diode (RD) line that is described in detail in the Sec. 2.2.1 [7].

- **3.3 V LDO.** No changes undergo from the 12 pixel ETTORE board, Analog De-

vices ADM7154ACPZ-3.3-R7 low-dropout regulator for the ASICs power supply. The ultra-low-noise LDO offers a total integrated noise down to 1.6 μV RMS from 10 Hz to 100 kHz, and its 600 mA capability can supply up to 7 ETTORE ASICs (it will be necessary for the 166 pixel ETTORE board) [7].

- **OUT channels.** Hirose FH29B-100S-0.2SHW 100-pin FPC connector for the output signals is a completely new structure compared to the one used in to the 12 pixel ETTORE board. It provides the 47 single-ended ETTORE outputs and 47 signal grounds [7].

- **Power and CTRL.** Hirose FH29B-100S-0.2SHW 100-pin FPC connector for the ASIC and SDD power supply, control lines, static bits and analog reference voltages. I have already said that it is a completely new connector compared to the previous ETTORE board prototype but the most important point to notice is that the majority of pins in this connector are free to accommodate the additional signals required in the 166 pixel TRISTAN module [7].

- **Other.** No changes undergo from the 12 pixel ETTORE board, The rest of the components on the PCB are mainly resistors and capacitors to implement passive filters for all the bias voltages going to the SDD cells and integrated JFETs [7].

2.2.4. 166 pixel ETTORE board

The 83-channel ASIC board is used in combination with the 166-pixel detector. The two ASIC boards needed for each module are identical and interchangeable. The number of channels almost doubled in comparison to the previous version (83 channels versus 47), maintaining the same PCB dimensions of 120 $\times$ 35 mm^2 and 1.6 mm thickness. However, to deal with the increase of signal density, both the number of signal layers and the size of the features, e.g. track width and via dimensions, have been reconsidered. Table 2.1 summarises the PCB feature modifications compared to the 47-channel and 12-channel versions.

PCB design rules comparison

	12ch ASIC B.	47ch ASIC B.	83ch ASIC B.
PCB area	$42cm^2$	$42cm^2$	$42cm^2$
Number of ASICs	1	4	7
PCB layers	–	8	12
Min.track width/spacing	$100\mu m^{(*)}$	$100\mu m$	$75\mu m$
Min. via hole size	$200\mu m^{(*)}$	$200\mu m$	$150\mu m$

Table 2.1: The PCB rules for the different 12-channel, 47-channel and 166-channels prototypes of the ETTORE board. ($^{(*)}$ the dimensions were not limited by the specification for the 12 pixel ETTORE board design but by the future 47 and 166 one)

The new ASIC board appearance and layout are shown in Fig. 2.34. Despite the total signal rerouting and the addition of three ETTORE ASICs, the board's building blocks are the ones already presented in Sec. 2.2.3.

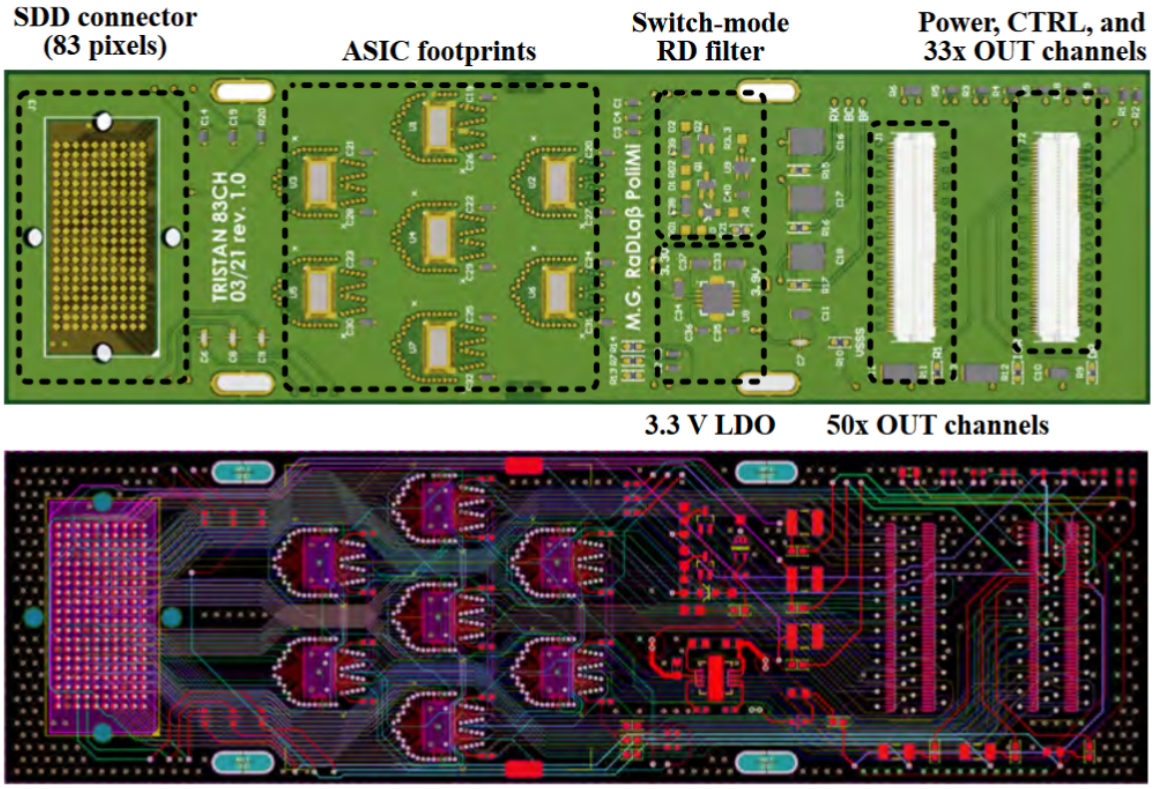


Figure 2.34: The 166 pixels ETTORE board [7].

90Mhz noise cancellation changes on 166 pixel ETTORE board

In the first semester of 2022, during the testing of the new 166 pixel detector, it was discovered by the MPP group a small 100 mV RMS noise signal at $\sim$ 90Mhz with high monochromaticity. This noise was found superimpose to the signal coming out of the ETTORE ASIC (all the channel had the same noise signal at the same frequency) (Fig. 2.35).

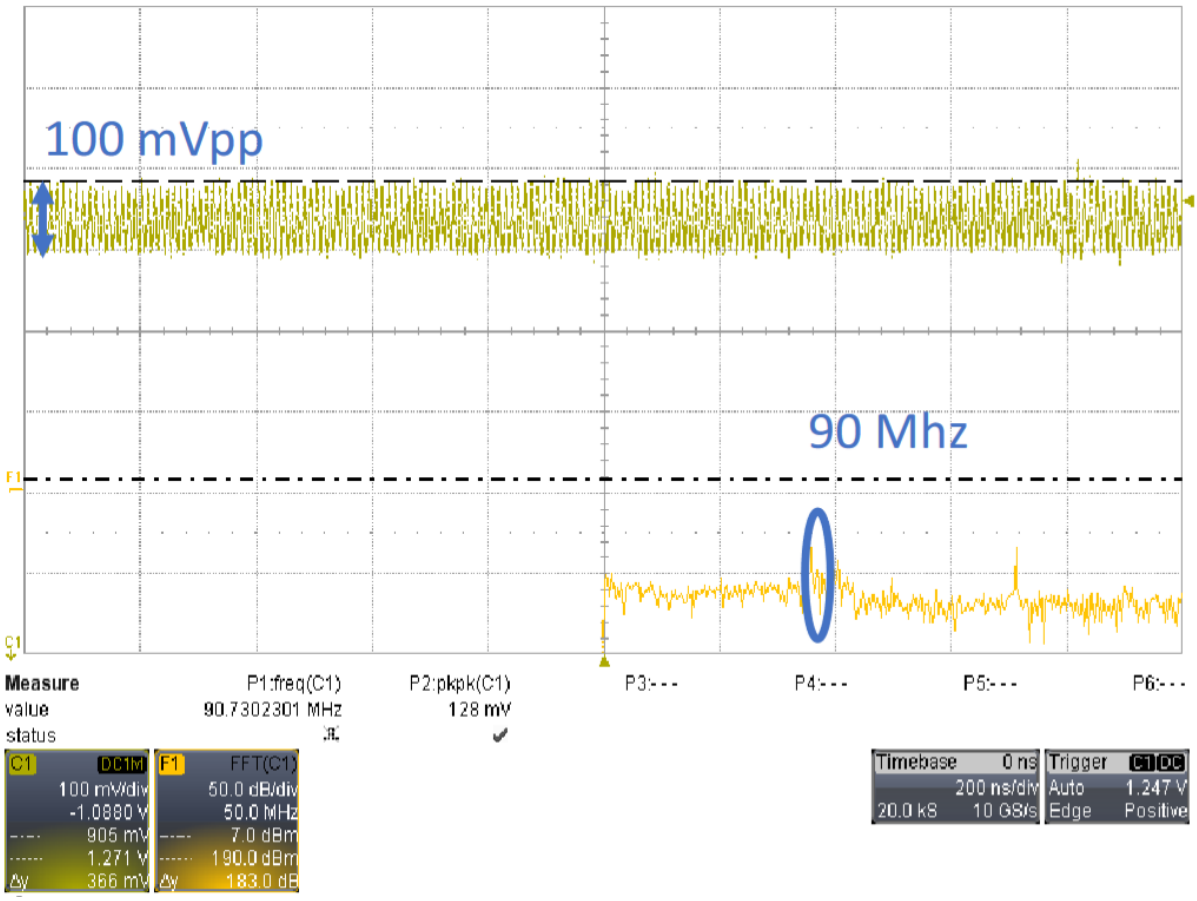


Figure 2.35: Image of the oscilloscope measurement on the output of one of the channel of the ETTORE board. The time and amplitude were Zoomed towards the visualisation of the 90Mhz noise signal (coming from the presentation of Daniele Manfrin on the solution proposal for the noise cancellation).

One of the possible causes suggested, for the 90Mhz noise, was the presence of some kind of instable loop coming from the novelty of using in parallel two ETTORE board for the same single detector (before the 166 pixel detector was used, there was only one ETTORE board per detector), but no strong theoretical explanation was found.
Instead, by trying to switch on and off different amount of ASICS (by forcing the output

of the ASIC channel to ground, the single channel stops to work thanks to an internal mechanism, better described in [7]), the signal noise of 100mV RMS started to decrease after a threshold of almost all ASICs off (The discover can be attributed mainly to Daniele Manfrin, Thesis student of Politecnico di Milano). This surprising discovery led to further tests and manipulations on ASICs until it was clear that the denominator in all the executed tests was the ASIC itself. Consequently, when too much ETTORE ASICs are in the same system, some instable loop that links all of them together makes the ∼90Mhz noise signal. after the establishment of ETTORE as cause of the noise signal detected, the designer of it (Paolo Trigilio of XGlab) started a circuit simulation to find the possible cause and The consequent solution. Finally the simulation suggested that the noise signal was in some way related to the V_{REF} signal line that was not filtered enough.
the final solution was to put, as near as possible to every single ASIC, a 100nF capacitor connected between ground and V_{REF} (take the Fig. 2.36 as a reference). The next step for the future would be to produce a new design for the board that includes this 100nF capacitor.

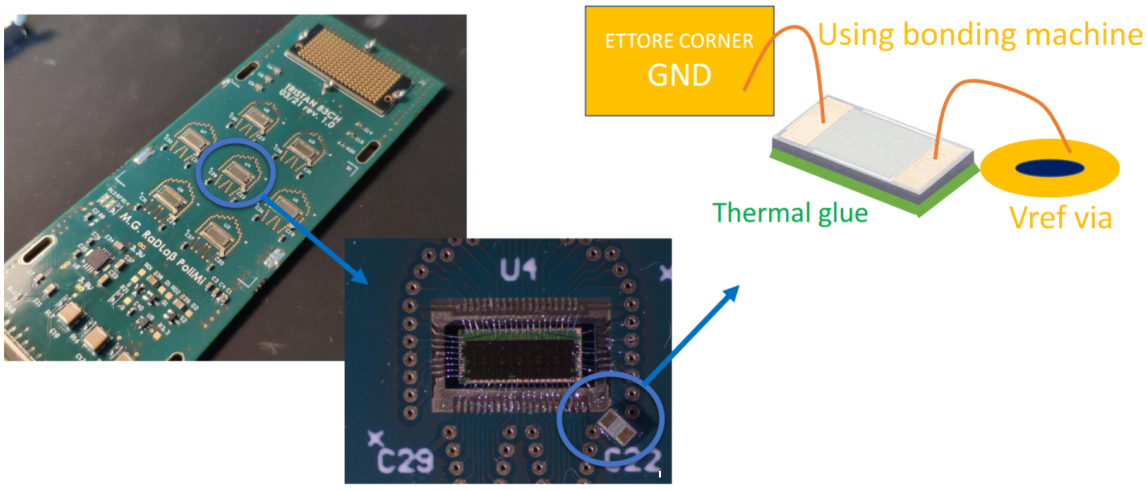


Figure 2.36: The 166 pixels ETTORE board with the capacitance from ground to V_{REF} near every single ASIC. The new capacitance of 100nF was introduced after the study to find the solution to avoid a little noise harmonic at around 90Mhz with 100mV RMS amplitude (this signal was discovered at the beginning of 2022 by MPP group). The study was conducted by Paolo Trigilio at XGlab through circuit simulations. The capacitance mounting and testing was done by us, the Politecnico di Milano Group in march 2022.

2.3. Bias boards

Here there will be a fast introduction on the main purposes of the bias board from 12 pixel setup to the 166 pixel bias board future evolution. The changes on the Bias board throughout the different evolution of the detector number of pixel will be highlighted.

2.3.1. 12 pixel XGlab Bias Board

Fig.2.37 shows the bias board, which is designed in collaboration with XGLab. The Board main functions are to provide the bias voltages and to reset signals to the SDDs and the ETTORE ASICs. The power supply used for this board is a 24 V bench top power supply and, thanks to its internal DC/DC converters, it generates all the voltages needed for the biasing of the detector, HV, BF , BC , V_{SSS} , V_D, IGR, R1, RX and the ones needed by the ASICs boards. Moreover, it is possible to make a manual adjustment of these voltages by using the resistive trimmers on the bias board [4]. In regard to the generation of the reset inputs on the detector and on the ASIC, there are three different sources that can be used :

- **Reset given by the ASIC**
  When one channel of ETTORE reaches its saturation point (V_{TH}) it is generated a positive pulse that reaches the bias board (SAT_OUT signal line). After that, the bias board generates two different reset signals, one for the ASIC and one for the SDD. These two signals are synchronized and their length is adjustable thanks to resistive trimmers. The voltages for the reset pulse of the detector are trimmable between -15 V and 5 V [4];

- **Periodic Reset**
  On the bias board there is an oscillator that gives the possibility to have a periodic reset. Its frequency depends on the values of resistance and the capacitance of the components connected on the astable circuit of the oscillator is set with a default period of 2 ms. To deactivate (activate) this periodic reset (that is the default one active on this board) a jumper has to be connected (disconnected) [4];

- **External Reset**
  Thanks to an SMA connector, it is possible to provide an external reset signal using a signal generator. This is the only reset mode that has been used at Politecnico di Milano [4].

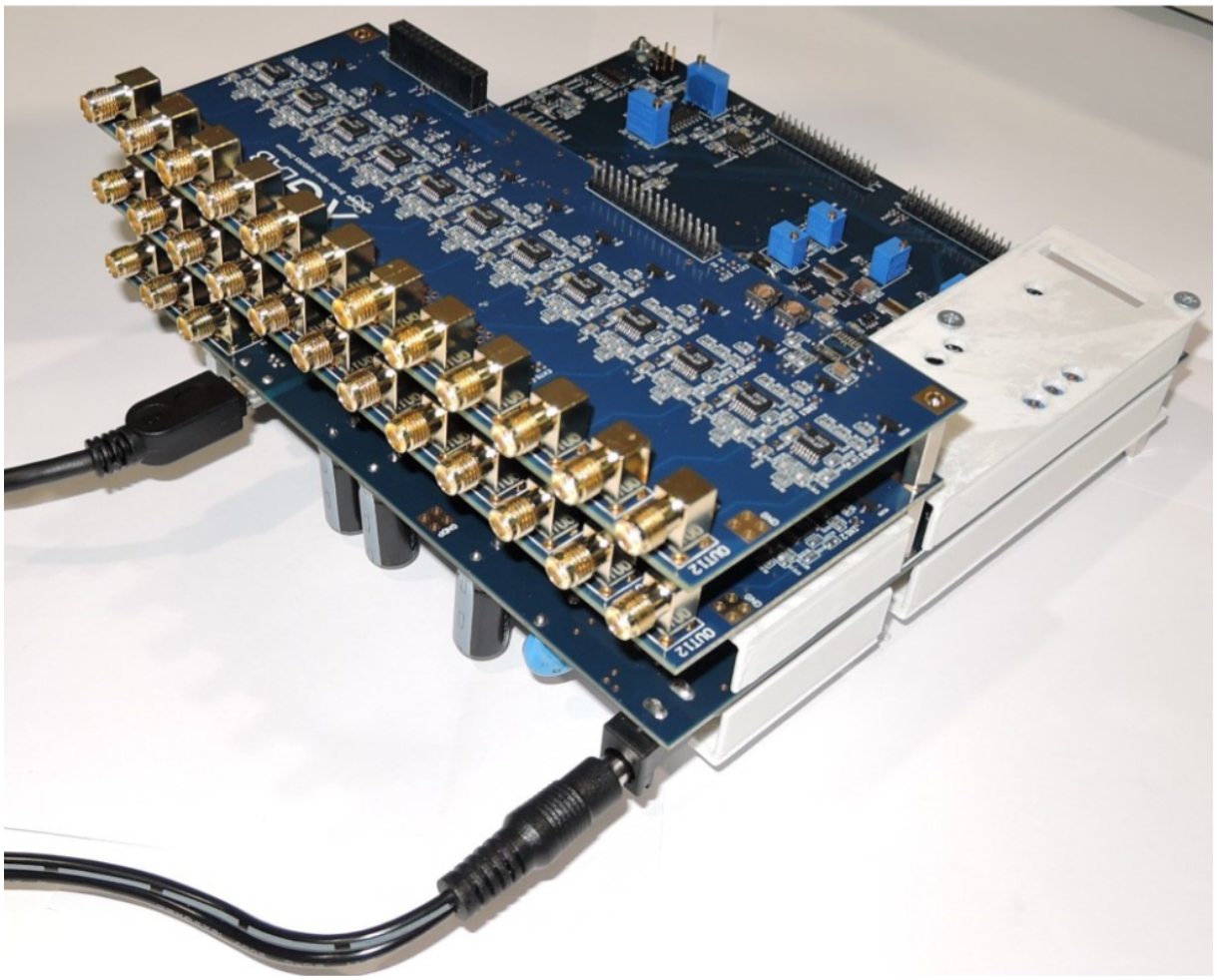


Figure 2.37: Bias Board developed by XGLab, structured for the 12 pixel detector setup. [4].

Using a custom software GUI (made by XGlab) it is possible to check and adjust some parameters without acting on the hardware:

- Activate or deactivate the High Voltage part of the Circuit (HV), and all the detector voltages derived from that;
- Check the temperature of the system thanks to a temperature monitor;
- Activate or kill specific ETTORE channels;
- Set the ASIC references voltages and static bits;
- Monitor the SDD's JFET current.

On the bias board all the ETTORE output signals are amplified by a factor of 2 to make

negligible the noise introduced by the following circuits [4].

2.3.2. 47 pixel XGlab Bias Board

As we can see from the Fig.2.38 the XGlab bias board has the same structure but an addition of only two more "floor" of boards for the buffering of the output of the ASICs channels.
(Notice that: because of the change with the FPC connector on the ETTORE board (Sub-Sec. 2.2.3), the setup required a board connector adapter from the FPC to the ribbon one of the XGlab bias board)

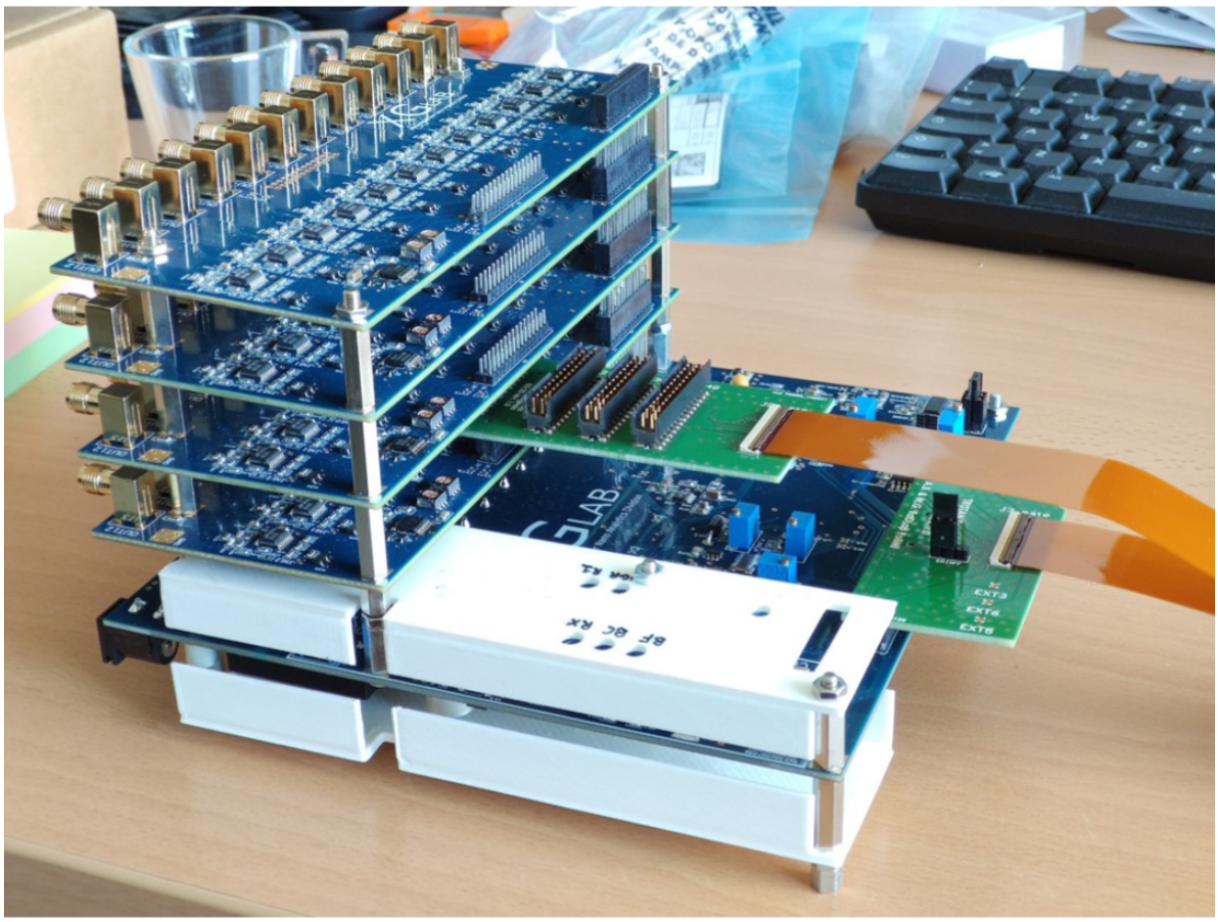


Figure 2.38: Bias Board developed by XGLab, structured for the 47 pixel detector setup. It has just two more board "floor" on top of the older 12 pixel bias board version [4].

2.3.3. 166 channel Bias Board

166 channel Alessio Pigliafreddo Bias Board

The Bias board for the 166 pixel detector was going to be produced by XGlab but Politecnico di Milano groups needed to have one earlier because the setup was ready (without considering the large cost to buy one more of the XGlab bias board). The Master Thesis of Alessio Pigliafreddo started to develop one (Fig. 2.39). Unfortunately, it was not enough reliable at the eye of the chief of the TRISTAN project compared to the new board that XGlab was already developing for the 166 pixel detector (based on the previous 47 channel bias board). In the end the Alessio bias board for the setup of the 166 pixel detector was used only by Politecnico di Milano group. Instead the MPP group waited to eventually use the newer and bigger XGlab bias board(Fig. 2.40).

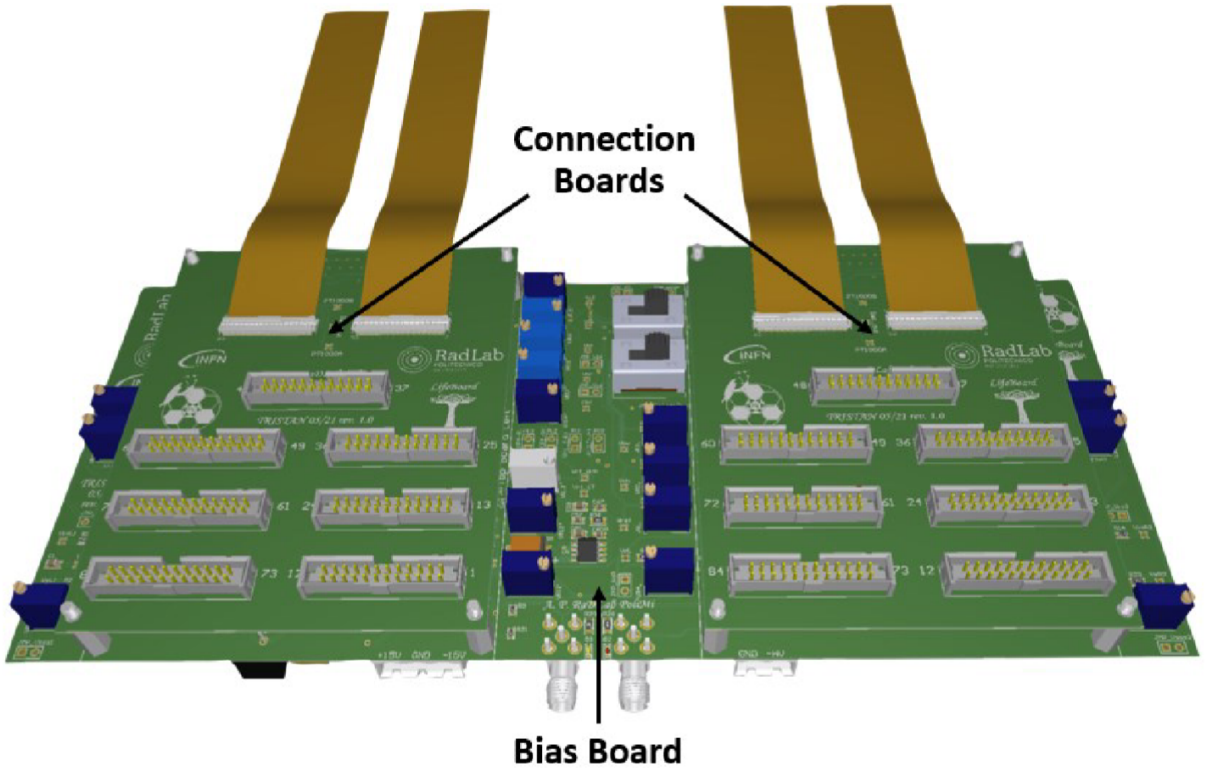


Figure 2.39: Bias Board developed by Alessio Pigliafreddo in collaboration with the PhD student Matteo Gugiatti, structured for the 166 pixel detector setup (photo coming from the Master Thesis of Alessio Pigliafreddo [16]).

166 channel XGlab Bias Board

The XGlab bias board for the 166 channel in Fig. 2.40 is a further evolution of the older bias boards employed for the 12 pixel and 47 pixel detector setups. It has the same working principle of the older versions but arranged to have 166 buffers for the outputs

of the ASICs channels and it is able to manage a higher power supply.

Figure 2.40: Bias Board developed by XGLab, structured for the 166 pixel detector setup (photo coming from the MPP 166 pixel setup presentation).

Recent Bias board news

A new 166 pixel Bias board is currently being developed by the Institute for Data Processing and Electronics at Karlsruher Institute for Technology (translated from "Institut für Prozessdatenverarbeitung und Elektronik" (IPE), "Karlsruher Institut für Technologie" (KIT)). The start of the development of a new Bias board was motivated by the definition of tighter constraint on the performance. Since the previous boards were no more able to satisfy the new limitations, the IPE group at KIT started to design the new Tristan bias

board.

2.4. ATHENA&KERBEROS and DANTE (DAQs)

This section will presents the capabilities of two DAQ system-types used in the TRISTAN project. There will be a brief confrontation between DANTE (DPP), a DAQ technology used in early stages of the TRISTAN project, and the ATHENA&KERBEROS system used after the 47-pixel detector technology; [11].

2.4.1. DANTE, earlier developed DAQ

Figure 2.41: 8-channel DANTE DPP developed by XGLab [4].

DANTE is a Digital Pulse Processor (DPP) produced by XGLab. It was mainly used in the 12 pixel detector test setup in the period of Alberto Brunero Thesis [4] (in 2019/2020).A photo of a single unit is shown in fig.2.41. This acquisition system uses a 16-bit at 125 Mhz ADCs on the incoming waveform and, by means of a trapezoidal shape digital filtering, it allows to acquire the energy spectrum from the detector signals. DANTE is connected to the PC through USB connection: with a dedicated GUI, it is possible to set the filter parameters and acquire spectra or save raw waveforms [4].

2.4.2. ATHENA and Kerberos Analog Pulse Processor

Athena is a Data concentrator platform based on a Xilinx Zynq UltraScale+ MPSoC Figure 2.43. Together with 4 Kerberos modules Figure 2.44, it is an Analog pulse processing (APP) architecture Figure 2.42. It creates the complete Data Acquisition and Readout system for the early phases testing of the final 166-pixel detection module of the TRISTAN project [11].

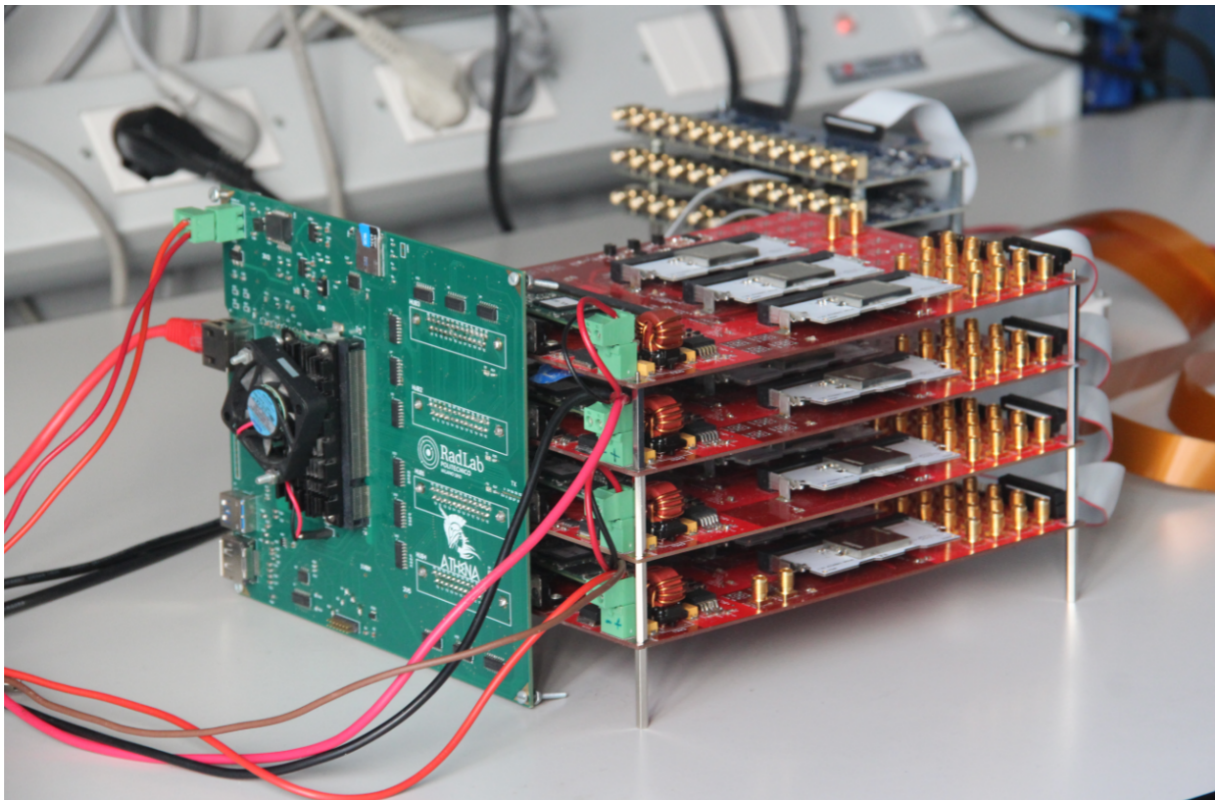


Figure 2.42: [11]

Athena collects the data arriving from the four Kerberos platforms and coordinates

the inter-Kerberos triggering. Each time any channel registers an event, all Kerberos platforms are read out simultaneously, producing a 192-channel frame ($16\frac{Channel}{SFERA-ASIC} * 3\frac{SFERA-ASIC}{Kerberos} * 4\frac{Kerberos}{Athena}$). The Athena system offers a very compact ($16 \times 22 \times 22$ cm3) and power-efficient (175 mW/ch) solution to readout large SDD matrices. It is in use, from the beginning of the first semester of 2022, in the phase-0 TRISTAN tests made in the KATRIN MoS with the 166-pixel module in 3D configuration [7].

ATHENA

Athena platform acts as global trigger and event builder for up to 4 Kerberos modules. Athena mounts a Xilinx Zynq UltraScale+ MPSoC module and communicates with the Kerberos platform via a custom AXI-4 Stream protocol for both transmission and reception. At hardware level, the connection between the two PCBs is done using DSUB-25 connectors. Instead, the output data is sent via an Ethernet port (RJ-45) located on the left side of the PCB. Gigabit Ethernet communication has been chosen as output data transfer method, thanks to its good performances in high EMI environments like the TRISTAN spectrometer, as well as its high bandwidth and its widespread availability in any commercial PC [11]. During the development process two version of the board were produced. The second version of the Athena board (Fig. 2.43) has a new layout that makes the final system more compact, mounting the four Kerberos directly on the back of the new system without the use of cables.

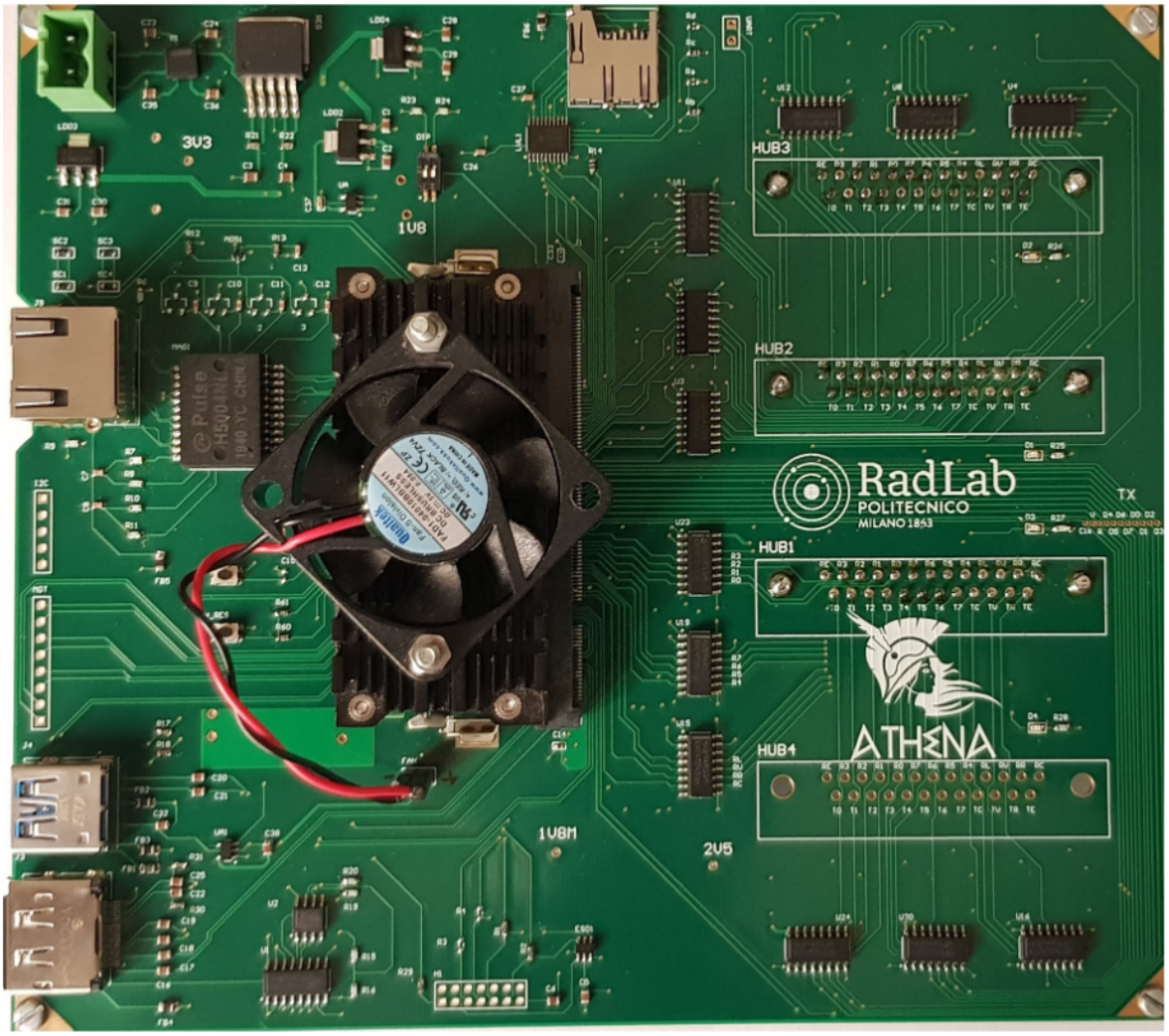


Figure 2.43: [11]

(For more details on the Athena system development and structures details I suggest to read the PhD Thesis of Pietro King [11])

Kerberos

The Tristan Project required the creation of an electronic back-end for the early readout of TRISTAN sensors, in order to characterize them and test its various configurations [11]. The characteristics that needed to be fulfilled were:

1. **A Large number of channels**, at least up to 47 channels.

2. **Independent readout of all channels** was needed to study charge sharing and

electron backscattering effects.

3. **100 counts/s/px** is the expected count rate for TRISTAN Monitor Spectrometer.

4. **300 eV FWHM @ 18 keV** is the target resolution for sterile neutrino discrimination.

5. **Modularity of the system** is necessary to read out the 166 pixels.

Given these design constraints, the choice between the development of a DPP or an APP focused on the latter. As a matter of fact, the main limitation was coming from the count of channels, which was very high for a completely digital system. Moreover, the count rate needed for the application was modest, and easily achievable by an analog pulse processor [11].
The fast prototyping and fabrication of the Kerberos platform analog solution permitted the testing of the TRISTAN detectors. In Fig. 2.44 starting from the left, the 48 analog inputs are connected to three analog pulse processors: SFERA (orange). Then the signals, after being processed and filtered by a semi-Gaussian Shaper, are stretched and buffered out. Subsequently, the outputs are digitized by the on-board ADCs (yellow). Finally, the FPGA (green) is used for signal regulation and external communication either via USB (purple) or a D-SUB 25 connector (blue) [11].

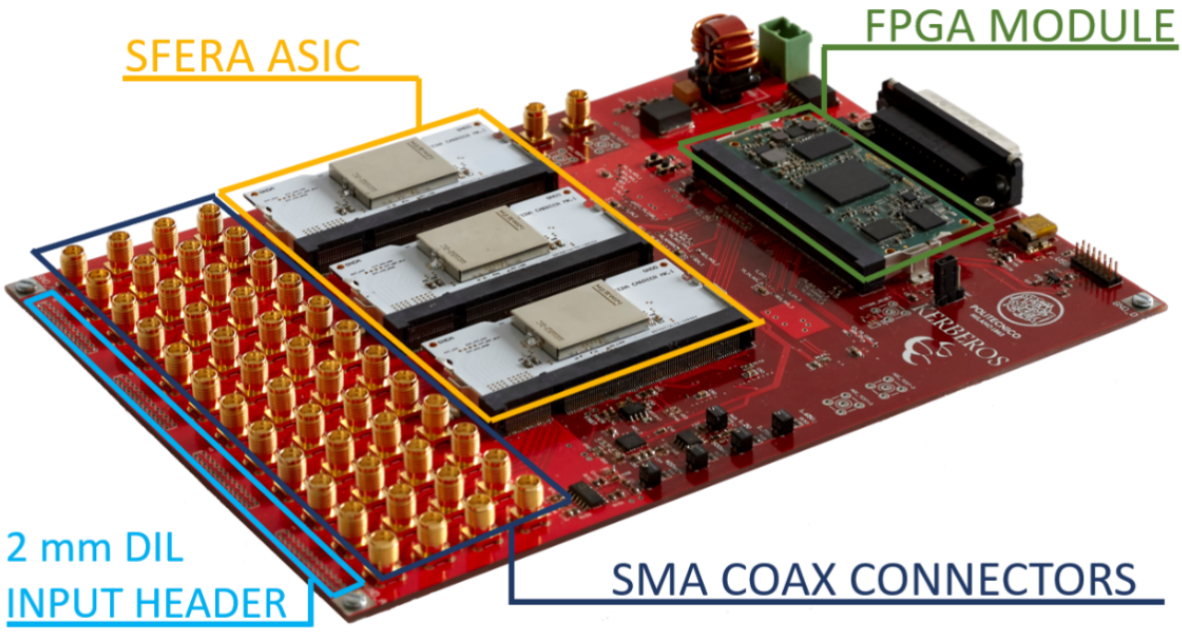


Figure 2.44: [11]

(For more details on the Kerberos system development and structures details I suggest to read the PhD Thesis of Pietro King [11])

2.4.3. DANTE (DPP) versus Kerberos (APP) DAQs

The comparison between DANTE and ATHENA&Kerberos DAQs was presented in an article on a new system of combined XRF and XRD techniques used to improve the analysis of excavated samples both in terms of selectivity and measuring time (PAiRED-X project at [5]).

In the beginning of the PAiRED-X project (Portable Analyzer combining fluoREscence and Diffraction of X-rays) the choice of a bench-top DPP was motivated by the versatility offered by digital processing, required in the early phases of the development of the system to optimize the detector operation. The DANTE DPP boards was available and was considered suitable for integration in the transportable instrument. However, if less bulky readout solutions was required, an alternative approach based on Analog Pulse Processing (APP) could be adopted. Interestingly, APP was demonstrated to be equivalent to DPP in terms of energy resolution [9] up to count rates of about 1 Mcps per channel. The Kerberos 48-channel APP readout platform was used to read-out the detector and make a comparison to DANTE [5].

The main difference between DANTE and Kerberos is the fact that one is a DPP system and the other one an APP. The advantage of an early digitisation of the signal, for DPP system, is the filtering action through digital processing and the recording of the signal shape. The digital filtering could be easily changed any time with changes in the code and information of the signal shape could be used for further analysis. Instead, the advantage of analog filtering and signal peak detection before the peak digitization, for APP systems, is the smaller area request for the same amount of channel of a DPP system and obviously a lower cost [11].

For the PAiRED-X project ([5]) there was an evaluation of the Kerberos APP system to discover if it is possible to have a more compact but still performing system. The comparison between DANTE and Kerberos, under the same parameters, obtained the same energy resolution. Considering the fact that a smaller DAQ system implies less components and less costs, the advantages, of using an APP system like Kerberos as the final DAQ, is self-evident.

3 | Testing Board and GUI for the ETTORE board

The Testing board, for the ETTORE Board, aims to verify the different channel preamplifier stages correct behavior, before connecting the detector to a damaged or not fully working board. Python GUI coupled with the testing board (connected to the PC via USB) enables the control of the testing procedure, the display of the test result, the creation of a Report file summing up if everything tested is working properly and handling the USB communication protocol.

3.1. What are the tests implemented

The Testing board has already been developed in the past by Alberto Brunero and Matteo Gugiatti, respectively ex master thesis and PhD thesis students. Their board was built to test only until the 47 pixel detector but the tests implemented are the same. Look at this Thesis for more details on the 47 channel testing board [4]

It is reasonable to think that the ETTORE board with such a large amount of channels could give some problem in the manufacturing process. Moreover the amount of boards that will be produced for the phase-1 and phase-2 of the TRISTAN project are 18 at first and then 24 more. It is quite obvious that probing manually 83 channels before placing the board on the TRISTAN setup would be misspent time, when a testing board could be made in less than a year to do the same job in order of magnitude in less time and surely with more accuracy. Therefore a testing board was already developed for 47 channel ETTORE board in 2019/2020 and then by me in 2022 for the 83 channel ETTORE board. The tests implemented are on the current polarization of the JFET (integrated on the SDDs), the right reset of the ASICs through a signal (called INHIBIT signal) and the CSAs response to an injected signal to its input.

3.1.1. JFET current polarisation test

This is a test on the current generators of each channel of ETTORE. Having a wrong current brought down by these generators would lead to problems on the polarization current single SDD integrated JFET, completely changing its working points. As we can see in Fig.3.1, this is mainly done looking at the voltage drop on a test resistor (the 10KΩ presented int the Sec.3.3), and converting this value in a current that the user can immediately see.

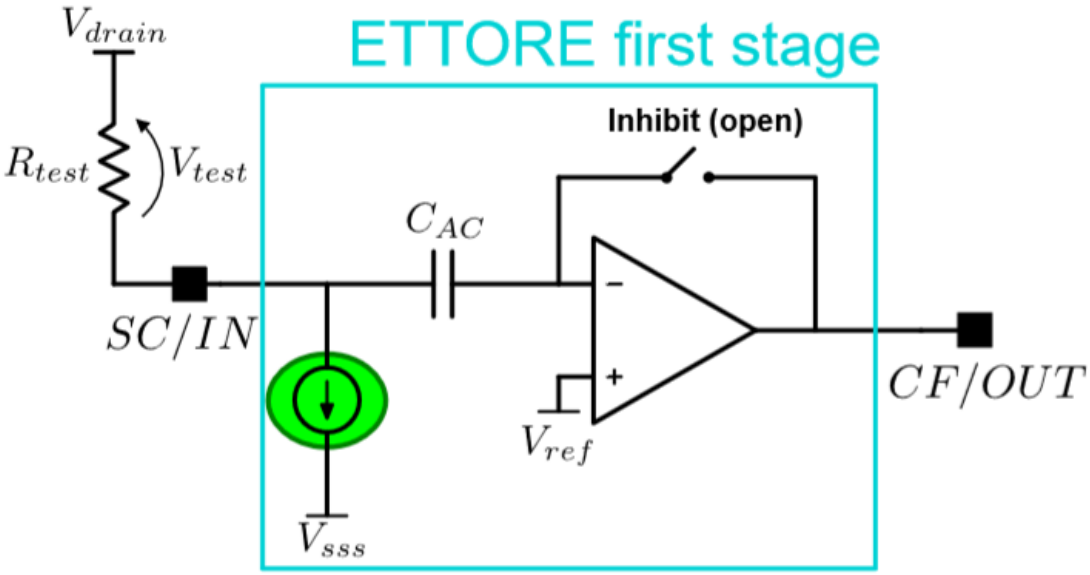


Figure 3.1: I_{SSS} test [4]

3.1.2. INHIBIT test

To check if the outputs of the ASICs are correctly bonded and that the amplifier is alive, the INHIBIT test is performed. Basically, applying a periodic INH signal to all the ASICs chanels, the output of the channels should saturate to 3 V when the inhibit is not active and it should goes to 0V when it is active. The periodic inhibit signal is generated in the μC of our board and sent to the ETTORE ASIC through the bias board first and the ETTORE board after. In Fig.3.2 a simplified schematic of this test is shown.

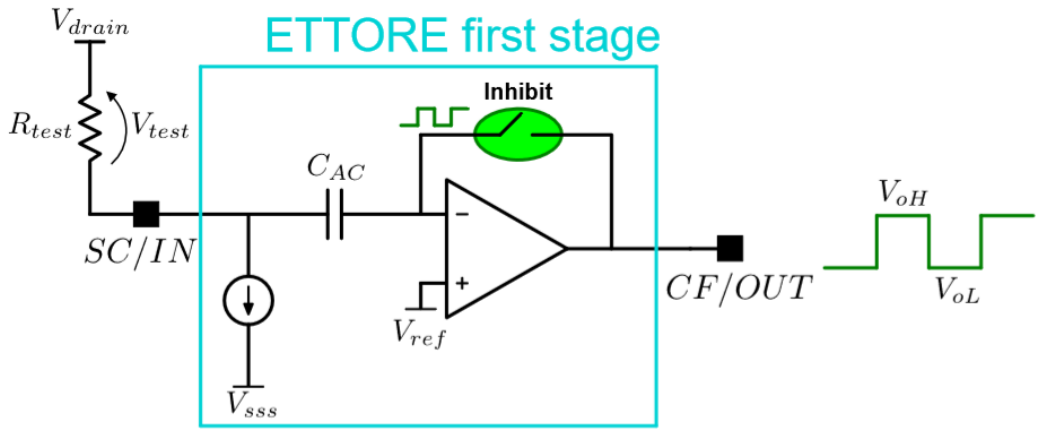


Figure 3.2: INHIBIT test [4]

3.1.3. Probe-Input test

To examine the behaviour of different channels individually, the injection test is performed. Having an external capacitor Ctest (20nF) connected to each input one at a time, a square wave is injected (ViH = 250 mV and ViL = 0 V), and the first stage of ETTORE, being in an open-loop configuration, acts as a comparator. When the square wave is applied, we expect a square wave with opposite slopes at the output, saturating at 3 V and 0 V. In Fig.3.3 the test representation.

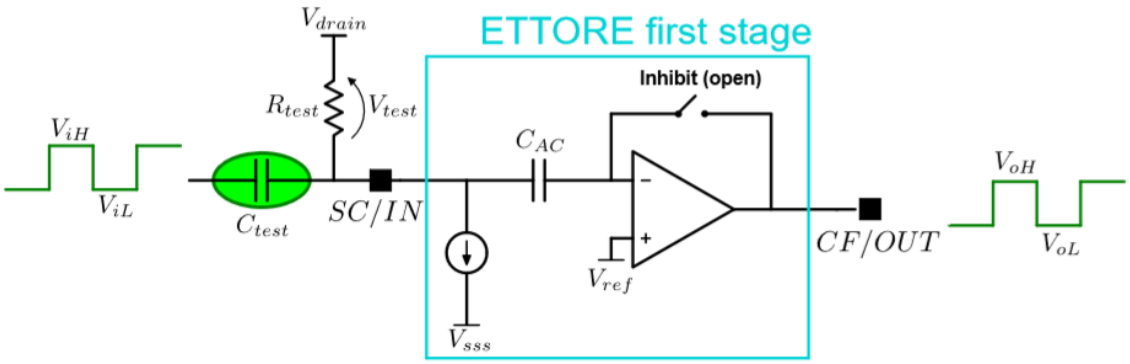


Figure 3.3: Probe-Input test [4]

3.2. Overview of the testing setup

From Fig.3.4 the schematics of the working principle of the setup its almost self explanatory. The ETTORE Board is biased (as it was already seen in Chapter 2 in the detectors

testing setups) by the 166 channel Bias board. Instead the Testing board is connected to the PC through USB and the power supply could be taken directly from the USB connection or eventually by a 3.3V-GND power generator (in Fig.3.8 you can see a three pin header near the μController that allows to make this selection with a jumper). Finally the Testing board is pressure connected with the ETTORE one, the GUI on the PC handles the communication and Testing procedure, the test results are collected and a Report file (on the correct behavior of the channel tested) is given. The Schematic view of the test procedure it's quite easy but obviously some setting requires a bit of shrewdness.

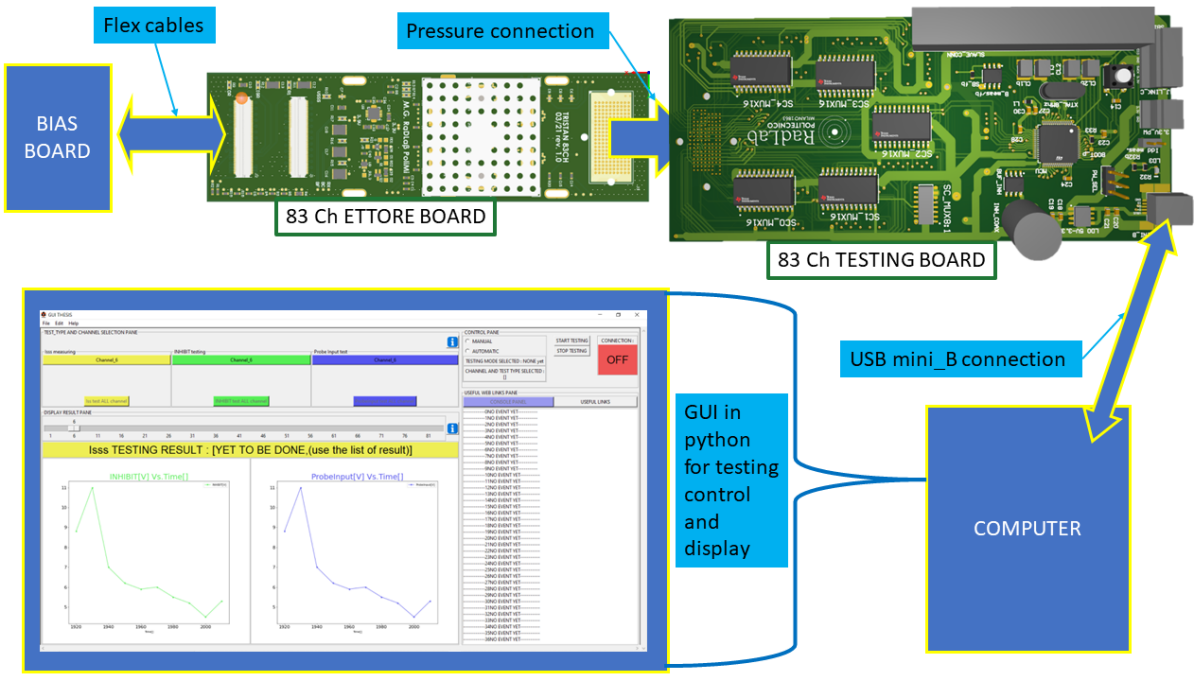
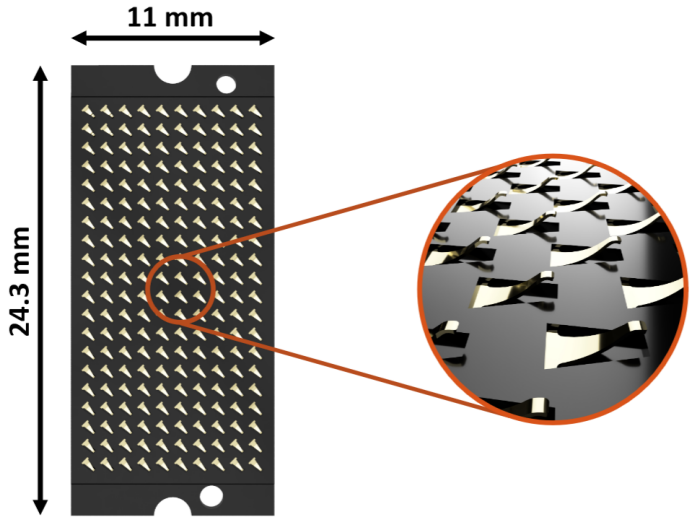


Figure 3.4: Testing board and GUI setup for the testing of the ETTORE ASICs channels

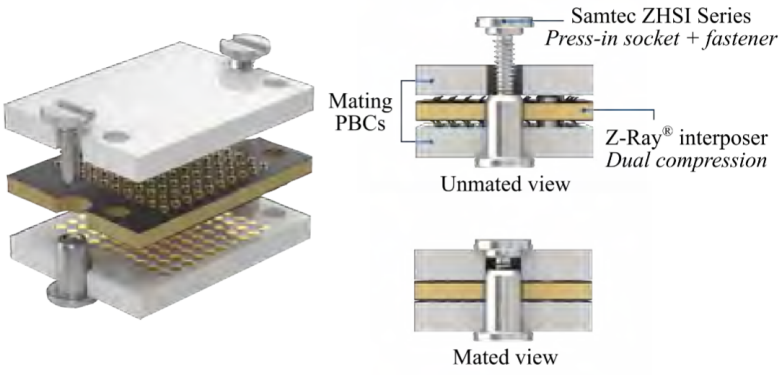
The Technical Details, for each testing component, will be presented in the next sections but the setup explanation is done here and with some more details on the more difficult steps. The delicate points in the testing setup are the pressure connection between the boards and then the INHIBIT signal coming from the Testing board to create an INH signal in the Bias board that will be used to reset the ASICs on the ETTORE board (there are trimmers on the bias board that needs to be adjusted properly).

The Board to Board Pressure connection already briefly presented in Sec.2.2.3, is done with the Samtec ZA1-20-2-1.00-Z-10 1-mm-pitch 200-pin dual-compression interposer (Fig. 3.5) and it requires a steady hand for its setting. The interposer needs to be put between the two areas of the testing and ETTORE board where the copper or gold

pads are distributed in a 200 pin (20 x 10) pattern. The way for positioning the interposer needs to follow the angle marks on the ETTORE board, near the 200pin pads. The two boards need to be positioned at two different planes and those planes would enable the boards to stay flat even after they are interposer-connected. Now there is the harder part: the interposer connection requires four quite small and fragile screws that need to be carefully screwed a little at a time until all of them are completely done. *(Note: the screws are very fragile and with a vigorous screwing it is easy to break them. The suggestion is to use only two fingers with the screwdriver and every screwing step should be of few turns and not too fast).*



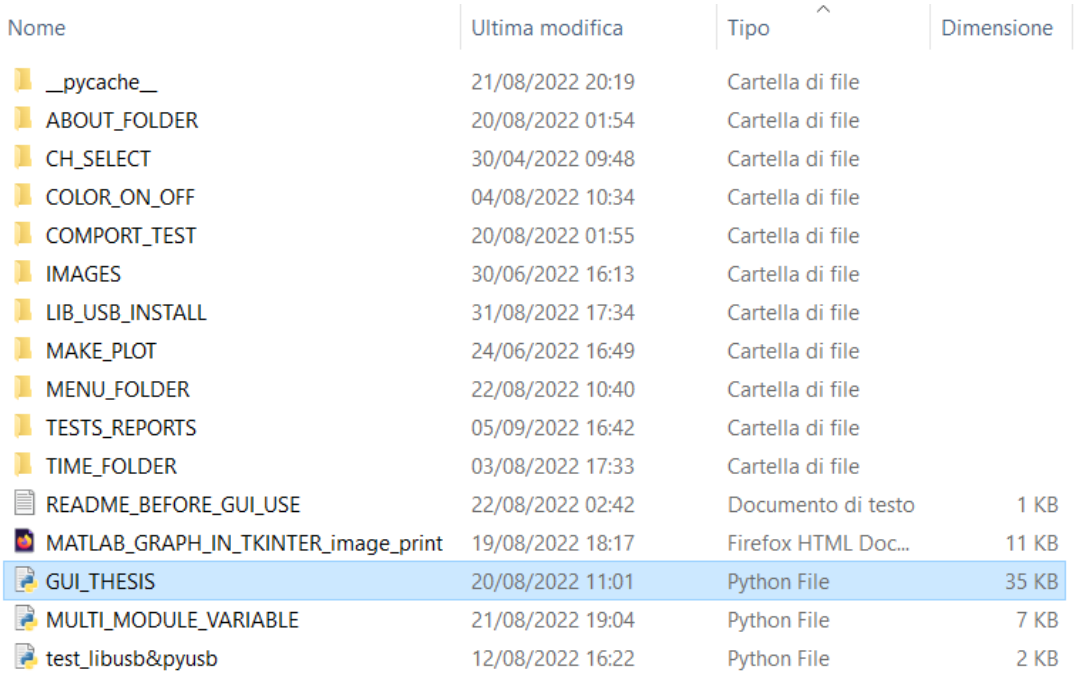
(a) Samtec ZA1-20-2-1.00-Z-10 1-mm-pitch 200-pin dual-compression interposer.



(b) Samtec ZA1-20-2-1.00-Z-10 with connection presentation [7].

Figure 3.5: Samtec ZA1-20-2-1.00-Z-10 interposer and the mounting image

For what concerns the **Testing board INHIBIT signal**, coming from the `BNC connector` on the testing board in Fig.3.8, it needs to be connected to the Bias board. This signal needs to be the substitution to the external periodic pulse signal (it is usually connected to the bias board in the detectors tests setups (Chapter 2)) to control the INH signal generated in the bias board to reset the ASICs on the ETTORE board. Unfortunately it is not as easy as only connecting the INHIBIT signal with a coaxial cable (with BNC connector) to the Bias board. In fact, to obtain a 50Khz 50% Duty-Cycle INH signal, at the output of the bias board, it is required to modify the bias board Trimmers that allows the modification of the INH (reset) signal Duty-Cycle.
(Note: the best way to adjust the trimmers on the bias board is to connect to the bias board the usually adopted signal generator for the detectors testing setups, but with a signal of 50Khz. Then with an oscilloscope connected to the INH bias board output, change the right trimmer to adjust the Duty-Cycle until 50% is reached).



Nome	Ultima modifica	Tipo	Dimensione
__pycache__	21/08/2022 20:19	Cartella di file	
ABOUT_FOLDER	20/08/2022 01:54	Cartella di file	
CH_SELECT	30/04/2022 09:48	Cartella di file	
COLOR_ON_OFF	04/08/2022 10:34	Cartella di file	
COMPORT_TEST	20/08/2022 01:55	Cartella di file	
IMAGES	30/06/2022 16:13	Cartella di file	
LIB_USB_INSTALL	31/08/2022 17:34	Cartella di file	
MAKE_PLOT	24/06/2022 16:49	Cartella di file	
MENU_FOLDER	22/08/2022 10:40	Cartella di file	
TESTS_REPORTS	05/09/2022 16:42	Cartella di file	
TIME_FOLDER	03/08/2022 17:33	Cartella di file	
README_BEFORE_GUI_USE	22/08/2022 02:42	Documento di testo	1 KB
MATLAB_GRAPH_IN_TKINTER_image_print	19/08/2022 18:17	Firefox HTML Doc...	11 KB
GUI_THESIS	20/08/2022 11:01	Python File	35 KB
MULTI_MODULE_VARIABLE	21/08/2022 19:04	Python File	7 KB
test_libusb&pyusb	12/08/2022 16:22	Python File	2 KB

Figure 3.6: the GUI folder for the THESIS

Instead, the other setup stages are quite standard as the introduction of this Section has presented them. The Bias Board needs to be connected, as already presented in the Chapter 2 for the detectors testing setups, to the ETTORE board with two Flexible Printed Circuits (FPC) (Sec.2.2.3). The GUI is opened on the Windows PC by clicking on the GUI_THESIS Python file in the GUI_THESIS folder (Fig.3.6). *(Inside the GUI_ THESIS folder a lot of different folders with Python modules inside were created by*

me to make different functionalities for the GUI.)

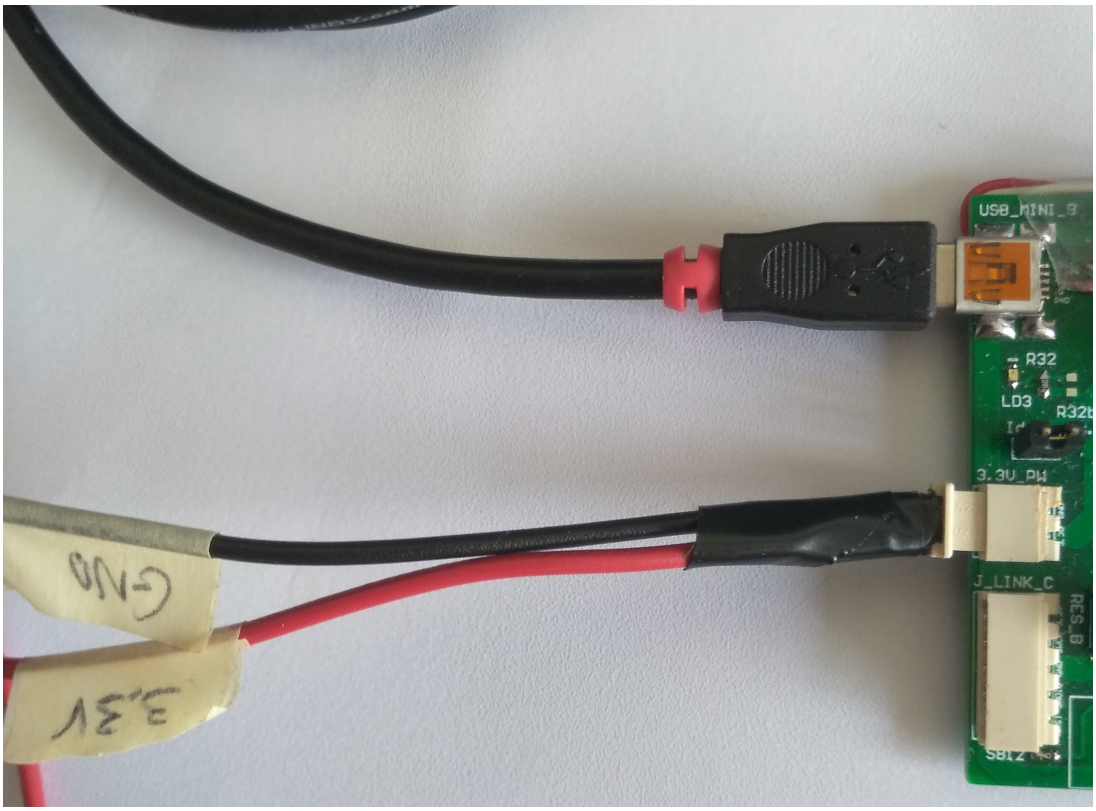


Figure 3.7: The photo has the testing board at the right and the two power supply cables in the middle. The Power supply are: the PC connected via USB (the USB is mainly used for GUI to board communication purposes) and the 3,3V-GND power generator

Then the USB cable with USB-mini-(B) is connected to the Testing board. *(Note :the letter (B) in USB-mini-(B) is used to point out that the USB-mini connector is from the device side and usually when the host side connector is not specified it is because it is the standard one USB-2.0-(A))*. I already said, at the beginning of this section, that the testing board can choose its power source from the 3 pin header with a jumper (on the board there is the drawing indicating how to make the choice). The USB (used mainly for communication between GUI and Board) and the 3,3V-GND power supplies connection are visible in Figure 3.7.

Finally all the setup is completed and you can start the testing by choosing what kind of test you prefer. Although there is the interesting possibility to display the test result in the GUI, some other options and settings can be useful for other testing related purposes. Now let's introduce the different parts that makes all this testing board work.

3.3. Testing board technical details

The Testing board has been designed with Altium (PCB design CAD). The entire master thesis started in march 2022 and the design began, after the self-training on different matters, at the end of May 2022. The board is 133 X 59 mm^2, is made out of 6 copper layers of signal connection separated by FR-4 (insulating PCB material). The high number of layers was required by the high area density of pads for the Samtec connector (Fig.3.5a). The board had the possibility to be larger and avoid the use of some layers, but because the $cost_{/area}$ of producing a board with 4 or 6 layers is the same, I had to take into account the area as a limiting factor. In fact the cost of a board is proportional to its area (obviously in other special cases other factors need to be take into account, like special materials, special treatments, area too dense of vias and others). All the design of the board was based around the most limiting PCB structure: the 200 pads for board to board connection. The fist component to be positioned on the Altium rendering of the board were the multiplexers, all component directly connected to the 200 pads. Then the second set of components were designed around the other high density pads component, the μController of the STM32 Family (STM32F303RET6). In the Fig. 3.8 and 3.9 we can appreciate the view of the component on the top and on the bottom of the board.

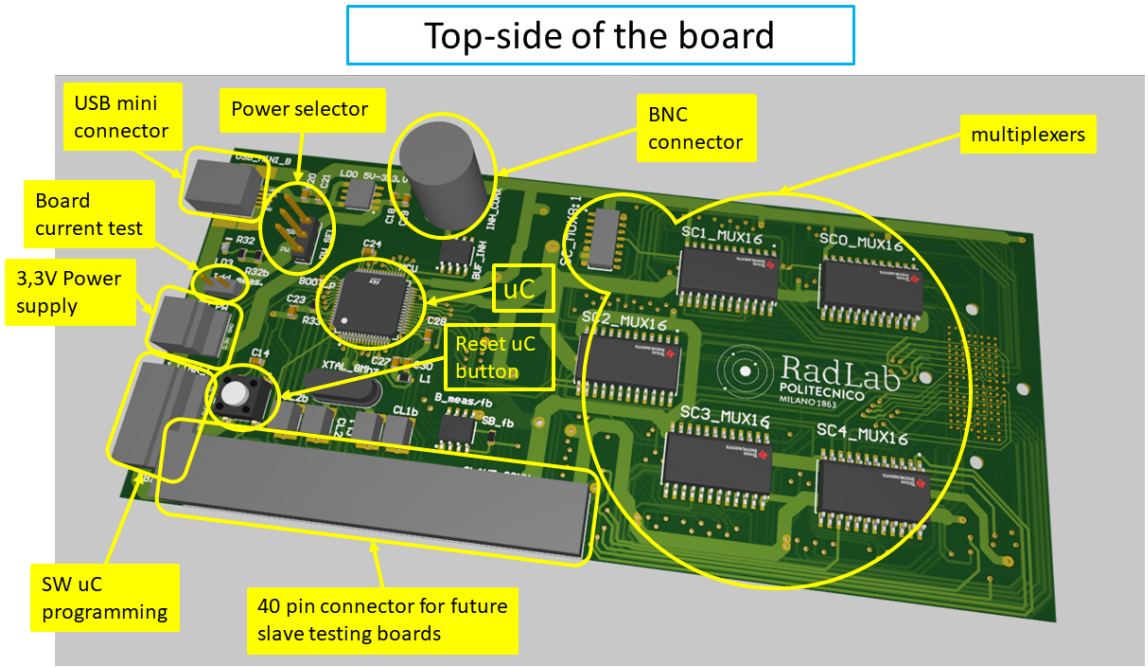


Figure 3.8: Altium Rendering of the testing board Top with description of the components

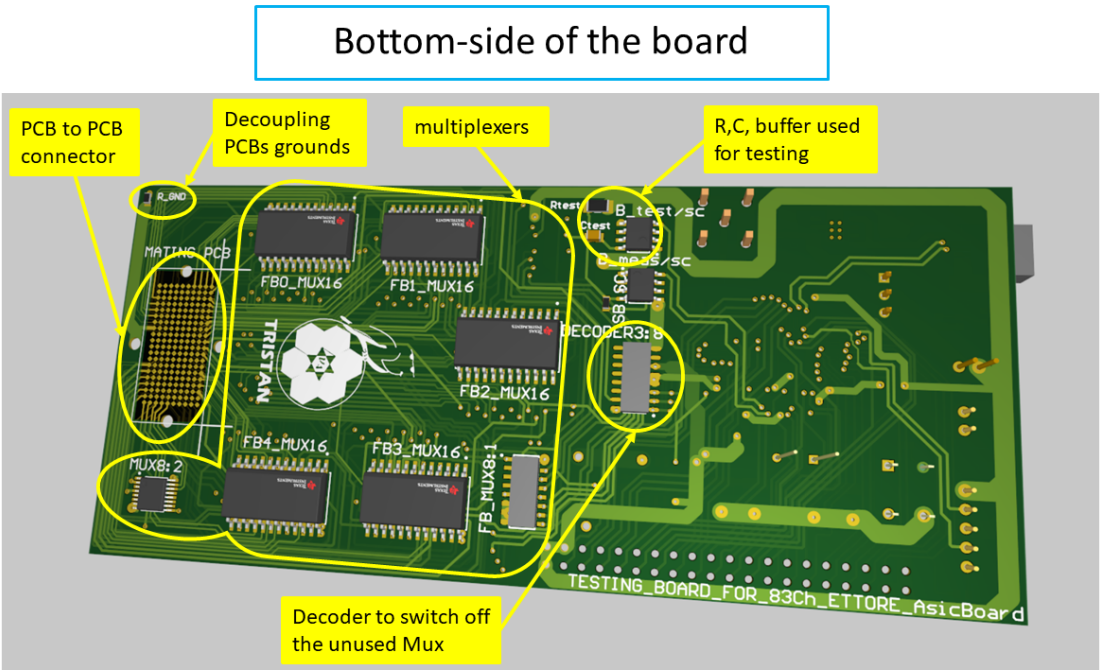


Figure 3.9: Altium Rendering of the testing board Bottom with description of the components

In the following there will a presentation of the component simplified by collecting them under the main working groups:

- **Multiplexing components:**
  The Analog multiplexers can be divided in two main groups. As you can see in the Fig. 3.10 there is the **SC** and the **FB** group. The two groups are not even on the same side of the board: one is on the Top and the other is at the Bottom. The division is made because each group is multiplexing two different kinds of lines entering from the 200 pads board to board connector area. The difference between the two types of lines could be self-evident by looking at the electronic schematics of one of the ASICs channel in the SubSec.2.2.1 Fig.2.31. The **FB** points are the outputs of the CSA of each ASIC channel, while **SC** points are the input of it. Because of this difference between the two points of the channel and because to test one channel we need to connect at the same time both **SC** and **FB** (belonging to the same channel) to the probing and acquisition structure on the testing board, the connection between Multiplexers is as it follows: I have designed two identical 84:1 2-row Analog-multiplexer for analog multiplexing 83 lines. I have designed the connection of six of the outputs of one 8:1 Analog Multiplexer to five 16:1 Analog

Multiplexer and one on half of the 8:2 Analog Multiplexer (you can appreciate it in the Fig. 3.10 in the **SC** or **FB** side).

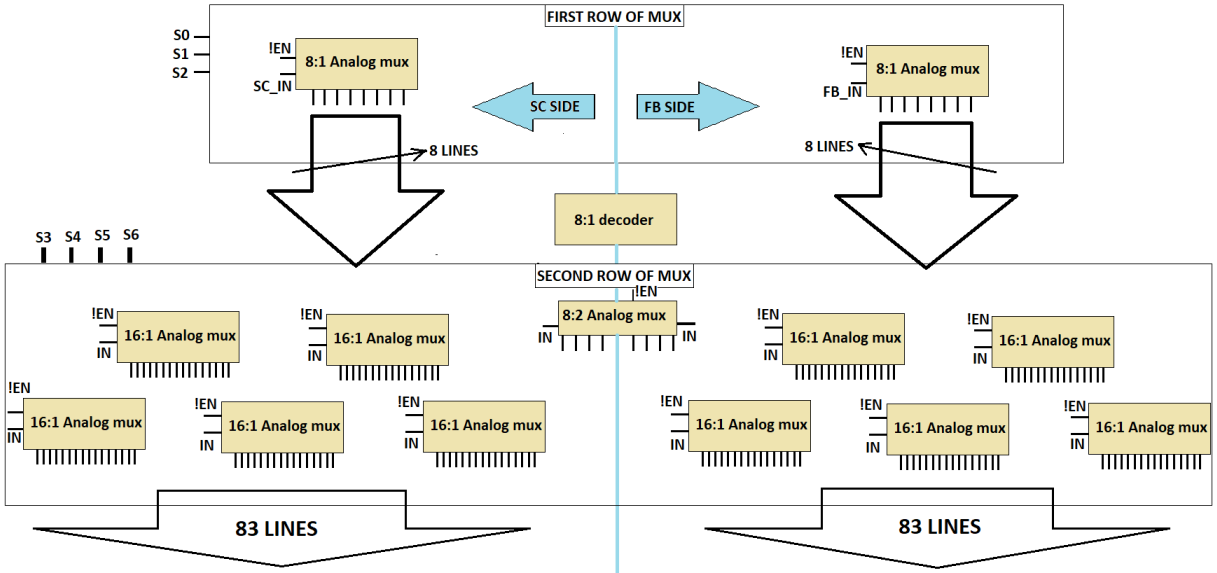


Figure 3.10: Schematic description of the Analog multiplexer connection

Because the IC Analog Multiplexers have the possibility to switch on and off through the **!EN** pin, I have used a decoder with the output pins connected to the second row of IC Analog Multiplexers. In this way the power consumption is decreased because the decoder activates only the Multiplexers of the second row that are currently connected to the testing circuitry by the first row multiplexer. Last but not least, the selector pins are partially connected to the first row (MSB selectors S0,S1 and S2 pins) the remaining part is connected to the second row (LSB selectors S3,S4,S5 and S6 pins) and the selector pins in the same row are connected in parallel to all the Multiplexers of the same row (look in the Fig.3.10 above). This selector pins arrive from the μController.
All the IC Analog Multiplexer are clearly visible in the Top and the Bottom sides of the board near the 200 pads area by looking at the Fig. 3.8&3.9.

- **Testing and acquisitions components:**
  The testing and acquisition circuitry is composed by 4 IC buffers, one 10KΩ resistance, one 20nF capacitance and the BNC (all visible in the two Fig.3.8&3.9 right

at the left of the multiplexers). Obviously some pins of the μController are used for the sampling, with internal ADCs, both the **SC** and the **FB** points coming from the two groups of multiplexers. Other two pins of the μController are used to produce a PWM signal at 50Khz with 50% Duty-Cycle that are used to create the INH (reset) signal for the ASICs on the bias board and to inject a test signal into the **SC** to see the response at **FB** of the ASIC channel CSA.

- **Power Supply components:**
  A brief discussion was already made in the previus section about the Power supply available (Sec.3.2), but some more details could be useful for the reader. The two power supply sources could arrive from the USB (5V-GND) cable connected to the PC or from a Power Generator with 3,3V-GND. The USB power supply is given by a 5V and GND lines with a max current of 500mA, then it is connected to a LDO with 3,3V-GND and max current of 500mA output(the whole circuit requires around 340 mA of current to work). The other power supply can be given by a Power Generator with 3,3V-GND and with probably much higher current limits compared to a USB cable connected to a PC. The selection between one supply or another is made by a three pin header visible in the Fig.3.8 in the top left over the μController (look in Fig.3.11 for more details). There is another 2 pin header related to Power supplied to the board. This 2 pin header has normally a jumper that let the power supply going around the board(Fig.3.11). This header could be used to connect an ammeter in substitution to the jumper and, after connecting the power to the board, to measure the current consumption. In Fig.3.11 there is a green led connected before the 2 pin header that signal if there are some power sources connected to the board.

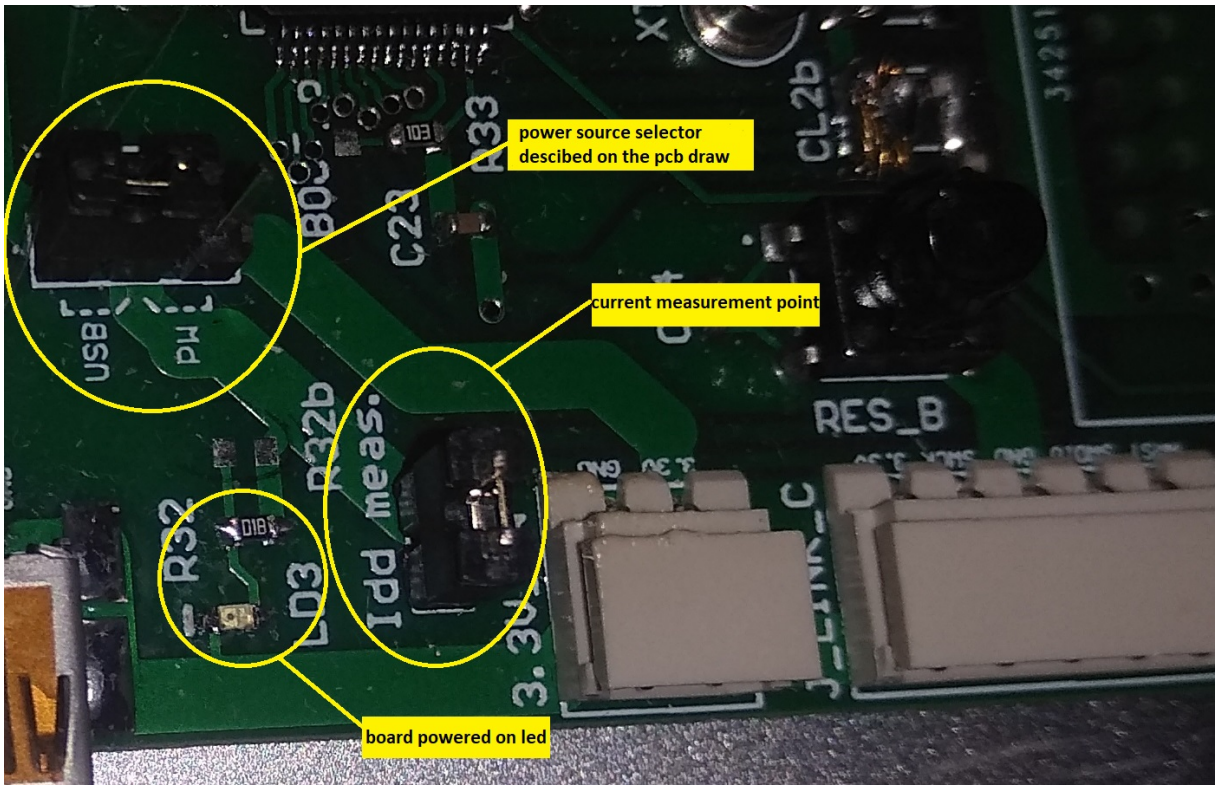


Figure 3.11: Picture of the power selector header, the current board consumption measurement point header and the green led that is on when there is power connected to the board

- **μController SW-programming, resetting, crystal resonator and USB communication:**
  Looking again to the left of the Fig.3.8 it is possible to notice the μController in the left-center of the board and other directly related components. On the top left there is the USB-mini-(B) connector that has its two signal line connected to the USB 2.0 OTG full speed (FS) interface pins (with speeds up to 12 Mbit/s) on the μC. Going down from the top left of the board, it is possible to see the reset bottom and the 5-pin connector for SW-programming the μController. The Reset button is connected to the NRST pin of μC: this pin allow to activate the resetting only if the GND is forced on it (this work is done by the reset button). The 5-pin connector allow the connection of the μC with its firmware reprogramming board (the ST-LINK board embedded on the NUCLEO board as in Fig.3.12).

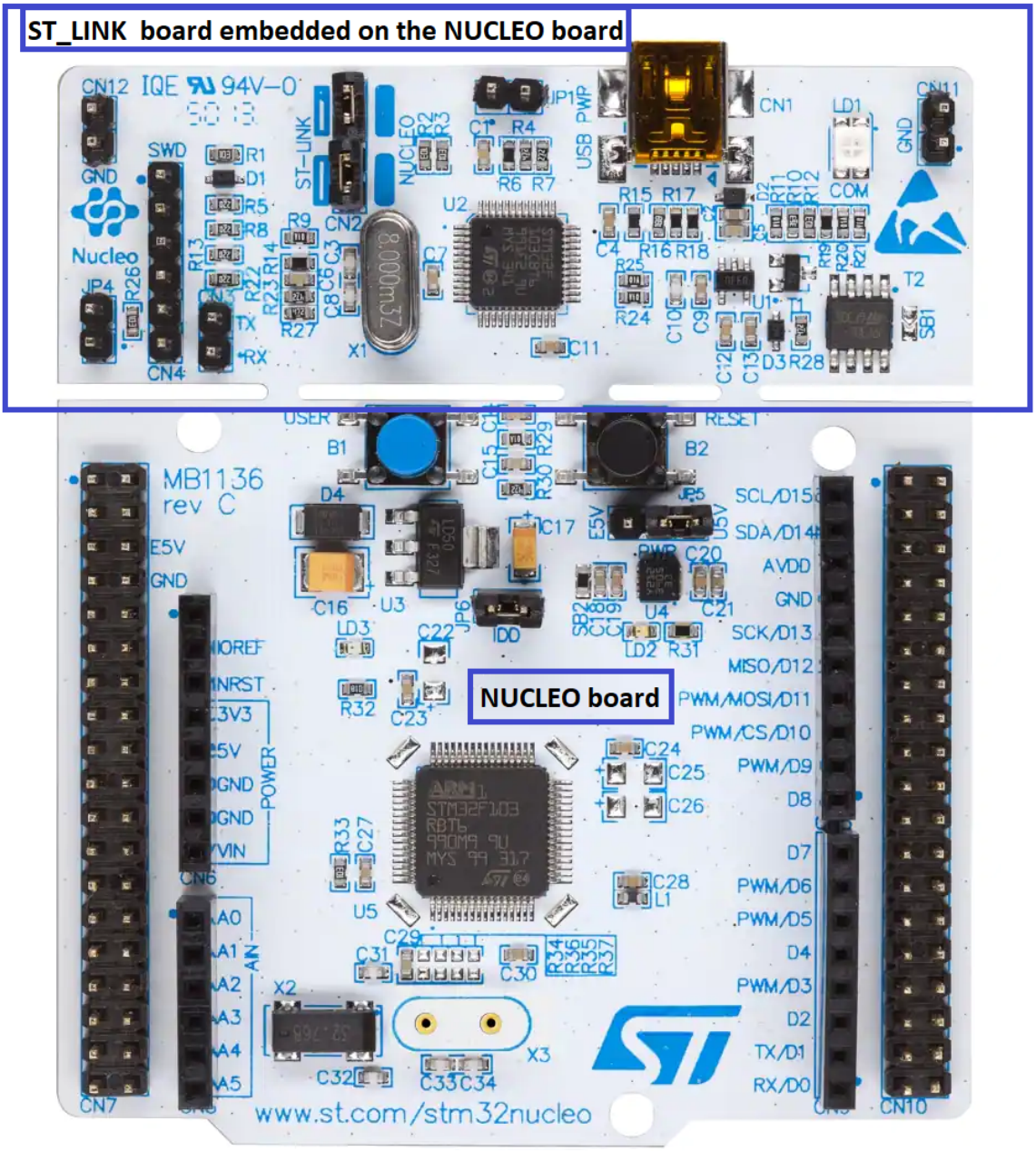


Figure 3.12: Picture of the Nucleo board with the embedded ST-LINK board (taken from the STM site:https://www.st.com/en/evaluation-tools/nucleo-f303re.html)

Finally, close to the bottom-left part of the board, the quartz crystal resonator (at 8Mhz) is connected to the μC with the relative capacitances. This allows to have an oscillator circuit that establish a sine wave at 8Mhz with ~few tens per million

frequency accuracy.
(Note: the capacitance associated with the oscillator circuit is no more the one represented in the rendering image of the board. The capacitances change was carried after noticing that the oscillation generated was not right. After some trials and errors I have established that the best solution would be three capacitances of 12pF per crystal resonator pin. For information on selecting the crystal and the capacitances values, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website (www.st.com). Instead the datascheet on the μC used, can be found in this link to the company site: https://www.st.com/resource/en/datasheet/stm32f303re.pdf)

- **40-pin connector for future board expansions:**
  This ribbon connector was thought in case future slave testing board would be developed to further test other feature of the acquisition system. More details will be available in the last chapter4.

It is worth to notice that this board is compatible with the old ETTORE board version until the 12 pixel one since, as I have already discussed in the Sec.2.2, the ETTORE boards after the one developed for the 12 pixel detector are all compatible and have the same size.

3.4. Python GUI technical details

The Graphic User Interface (GUI) has been developed with the Tkinter module that come with the installation of Python. The GUI is a window with very simple menu with limited options. The function available are: connecting the GUI via USB to the testing board, selecting the testing procedure that the user prefers, displaying the testing and communication with the board on a console, displaying the three test results for one channel at a time, producing a Report file that defines which channel have passed which test and connects to useful links and documentations that can help with the use of the GUI or the testing procedure.

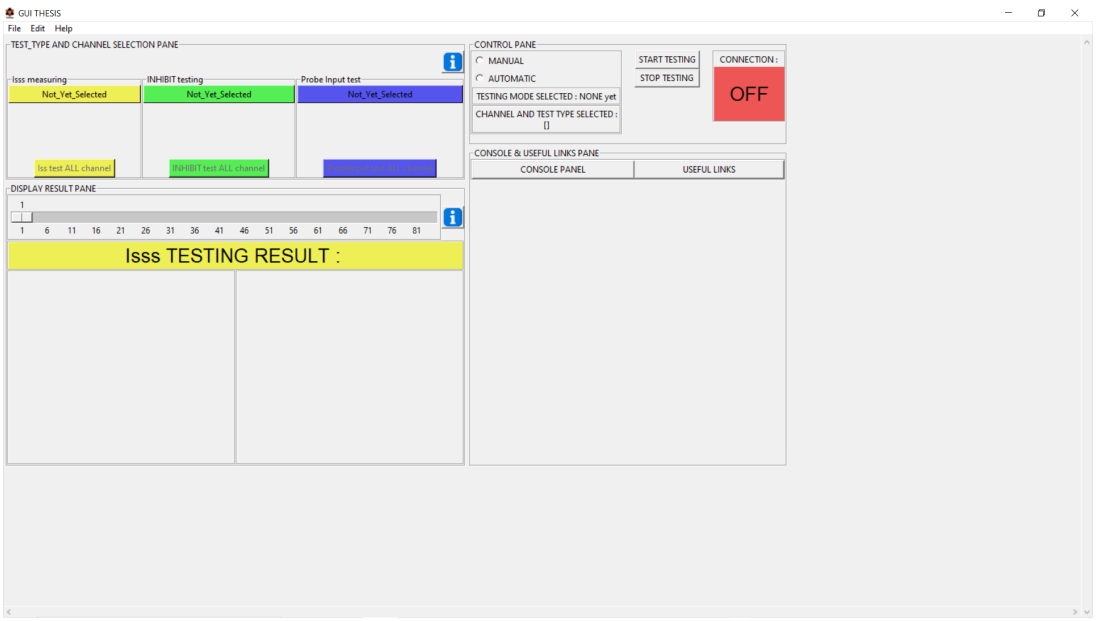


Figure 3.13: This is how the GUI looks like right after it is open

The GUI structure adopted the so called PanedWindows that allows the human interface sizing of the 4 different panes. The panes are labelled in their top-left part as it can be seen in Fig.3.13.

- **TEST-TYPE AND CHANNEL SELECTION PANE:**
  This pane contains an information button on the top-right that would open a little window with all the easy to use information of this pane and some other information on related functions on other panes. The other objects are collected under three frames (for the three tests available). Each of this frames are composed of setting for one of the three test available. Every single frame contains the selection of: at the top a single channel (between the 83 available) and the frame associated test, otherwise at the bottom all the channels and the frame associated test. The general idea is to add the possibility, in the case the user wants to test only part of the channel with only part of the test available, to have different choices of test procedure.

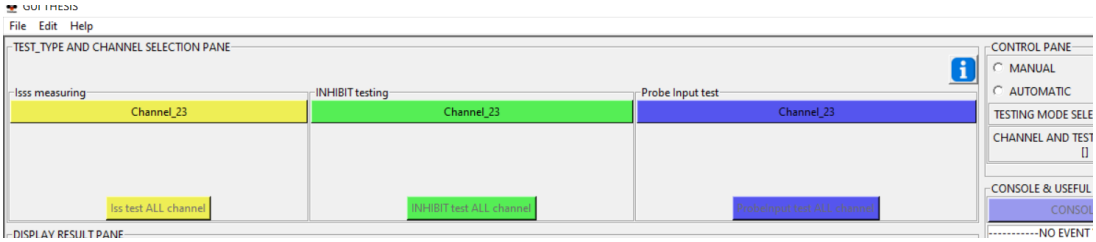


Figure 3.14: Pane that offer the choice between different types of manual test

(e.g. if I would like to test all the channel for the I_{SSS} test and only the 19^{th} channel for the INHIBIT test, I need to do this: search in the "TEST-TYPE AND...." pane, enter in the "I_{SSS} measuring" frame and click on the button at the bottom of the frame(I_{SSS} test All channel).The I_{SSS} test is done. Then for the 19^{th} channel INHIBIT test, search in the "INHIBIT testing" frame then click the button at the top of this frame, select the 19^{th} channel and finally click "START TESTING" in the "CONTROL PANE" pane. Then the INHIBIT test is done.

- **DISPLAY RESULT PANE:**
  This pane is very simple and can be appreciated in the Fig.3.15 right below. There is the information Button which is similar to the one of the pane described above, a scale to select the channel to be displayed, and then space for displaying the three test results.

Figure 3.15: Pane displaying the result with the scale to select the channel tests to be visualized

- **CONTROL PANE:**

This is the pane for handling the testing procedure and have information on the connection status. As his name states it is the Control pane and could be seen as the more related to the testing management. By looking at the Fig.3.16, we can identify three separate group of objects. At the left there is the selection through RadioBut-

tons for "MANUAL" or "AUTOMATIC" testing mode. (The AUTOMATIC mode test all the channel for all the three tests, instead the MANUAL mode requires the selection of which specific tests and/or channels you want). Under the mode selection there are two text labels that are used to indicate the mode selected and the last channel&test selected in the top-left pane. In the center of this Pane there are the simple "START TESTING" and "STOP TESTING" buttons. The last object is a squared Label addressed to function as a USB connection status indicator (using red and green color and OFF and ON text).

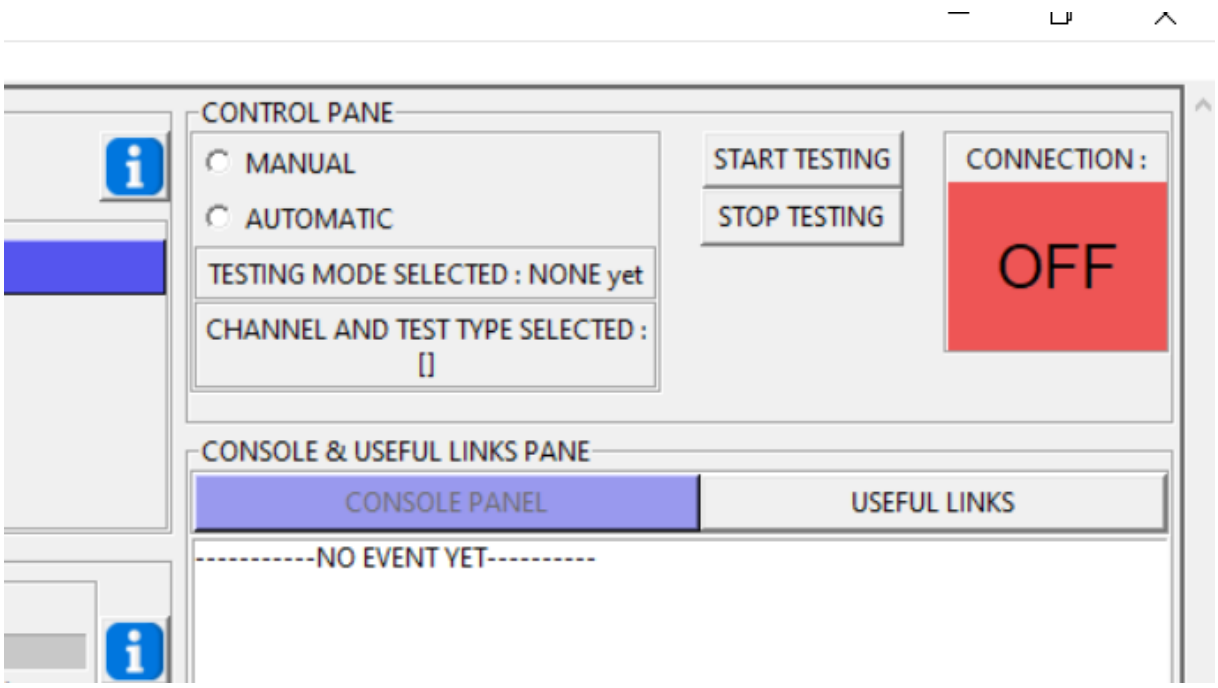


Figure 3.16: Pane that controls the choice of tests that can be made (with manual and automatic selection), the start and stop button for the test procedure and the connection to the board square indicator (red if OFF and green if ON)

- **CONSOLE&USEFUL LINK PANE:**

This last pane has two purposes visible one at a time. The CONSOLE purpose is to display the test and communication procedure during test time. Instead the USEFUL LINKS purpose is to make available different links and documentation related to the testing project or more in general to the TRISTAN project.
In Fig.3.17 the CONSOLE option is selected and it displays the test done and the communication exchanges between board and GUI. For example in the Figure is possible to see all the step that a test procedure required, in particular the Figure

below represent the AUTOMATIC test procedure:

1. **| TIME : 11:02:37 | ——-TESTING PROCEDURE BEGINS——-|**:
   it indicates that the board is connected and is working properly (this check will be better explained in the next Sec.3.5). A signal with the test information is sent to the board.

2. **- AUTOMATIC TEST SELECTED**
   *** TYPE : ALL channels for each single test**
   # **TEST : ALL the tests**
   # **CHANNEL : ALL the channels**:
   These are description of the type of test selected and requested to the board.

3. **| TIME : 11:02:37 | ——-THE BOARD RECEIVED THE COMMAND TO START THE A0 TEST——-|**:
   This means that the board has received the testing request, has started the selected testing procedure and has sent back a confirmation message that indicates what test procedure had received.

4. **| TIME : 11:02:37 | ——-THE BOARD FINISHED TESTING AND IS GOING TO SEND DATA COLLECTED——-|**:
   The board sent a message that indicates that it is ready to send the collected data to the GUI and that it still contains the information on what kind of test procedure has been used.

5. **| TIME : 11:02:37 | ——-TESTING PROCEDURE FINISHED——-|**:
   All the data has been collected and stored by the GUI and the communication for handling the testing procedure with the board finished. This happens when all the data that the testing procedure is supposed to produce is received (otherwise in a few seconds a new request for repeating the testing procedure would be send). Now the board goes back in its "idle" state where it is waiting for a new testing request to come.

6. **| THE TESTING PROCEDURE LASTED FOR [ms] : 400.79345703125|**:
   This test duration is considering the starting time as the clicking of the start of the test and the finish when all the data are received.

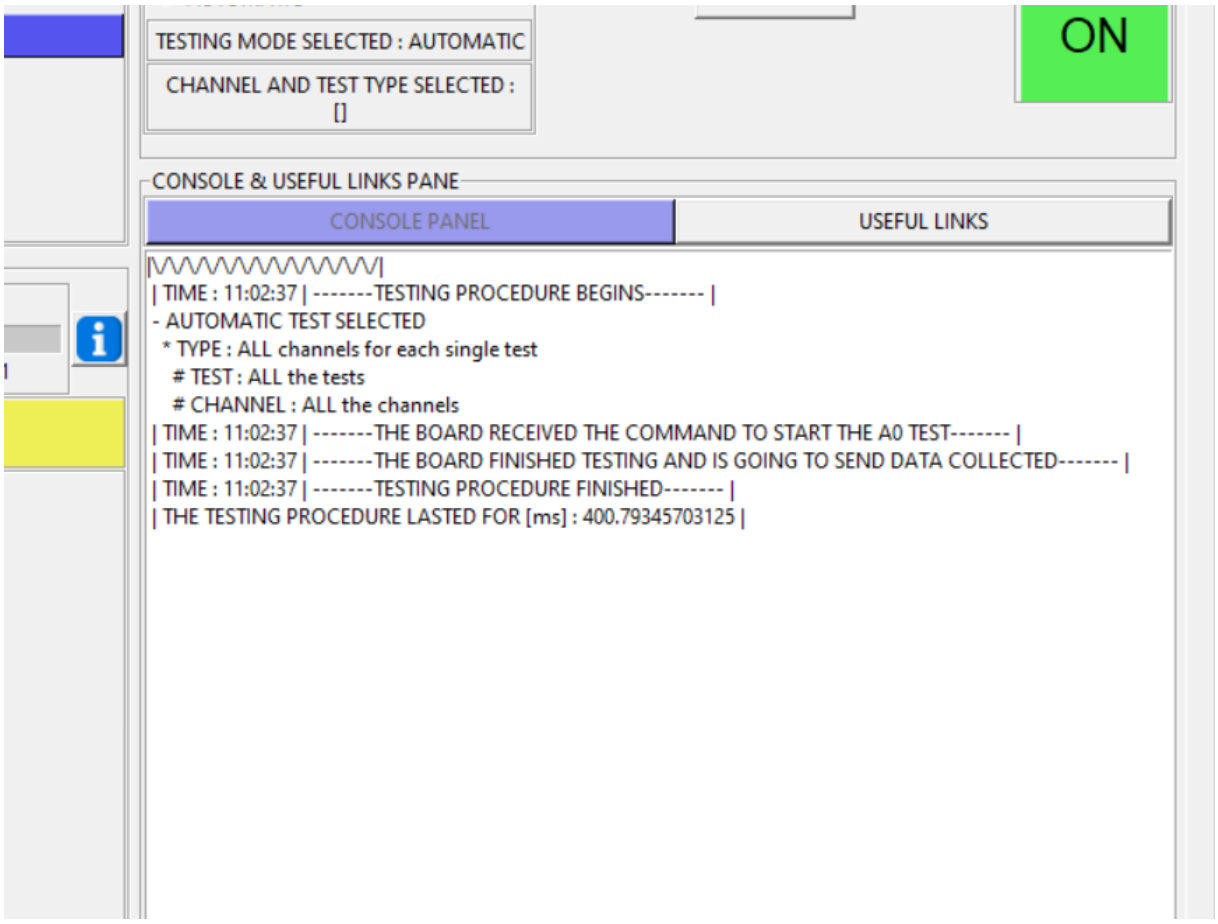


Figure 3.17: The Pane has the CONSOLE open to display the testing procedure advancement to register which test was done and how it went

Instead the USEFUL LINKS option allows to have the ready to use documentation of the board, the link to the Politecnico di Milano site, the RadLab presentation site and the TRISTAN shared-cloud space.

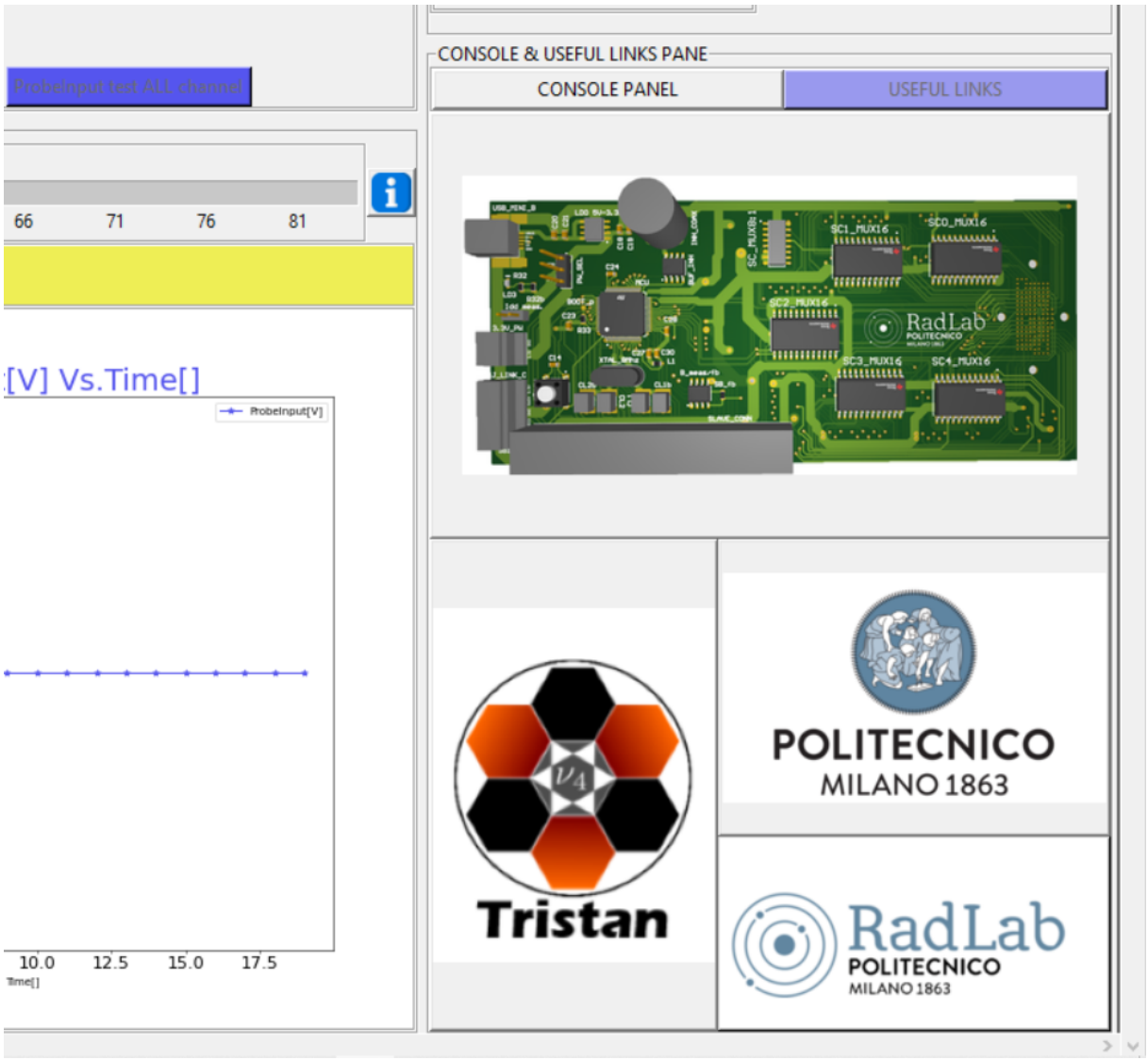
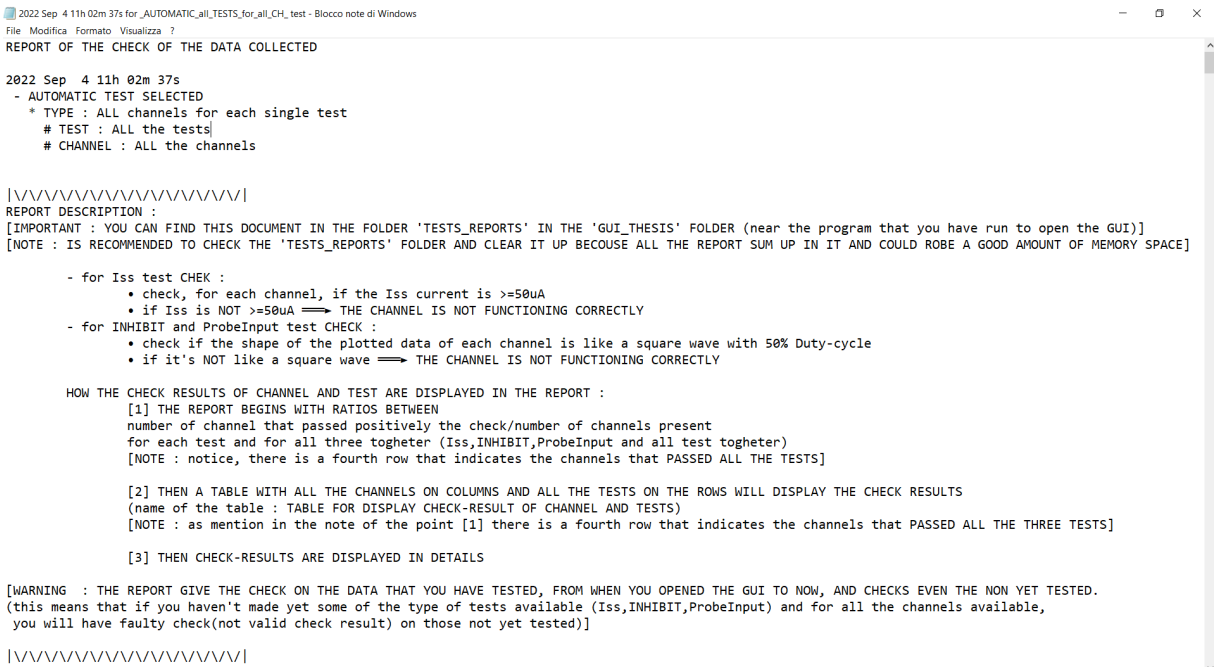


Figure 3.18: Pane contains different buttons that connect to useful links and documentation. The image displayed over them represents what kind of information could be found

After every test procedure ends a REPORT text-file is produced with all the cumulative and detailed result on which channels are working properly and which are not. Every REPORT indicates what is it (in the Title), when it was done and after what kind of test procedure it was produced. It always contains the introduction on what are the checks done on the channels tests data and how the results are displayed. In the fig.3.19 below there is an example of the first part of the REPORT file produced after an AUTOMATIC test procedure.



2022 Sep 4 11h 02m 37s for _AUTOMATIC_all_TESTS_for_all_CH_ test - Blocco note di Windows

File Modifica Formato Visualizza ?

```
REPORT OF THE CHECK OF THE DATA COLLECTED

2022 Sep  4 11h 02m 37s
 - AUTOMATIC TEST SELECTED
   * TYPE : ALL channels for each single test
     # TEST : ALL the tests
     # CHANNEL : ALL the channels


|\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/|
REPORT DESCRIPTION :
[IMPORTANT : YOU CAN FIND THIS DOCUMENT IN THE FOLDER 'TESTS_REPORTS' IN THE 'GUI_THESIS' FOLDER (near the program that you have run to open the GUI)]
[NOTE : IS RECOMMENDED TO CHECK THE 'TESTS_REPORTS' FOLDER AND CLEAR IT UP BECOUSE ALL THE REPORT SUM UP IN IT AND COULD ROBE A GOOD AMOUNT OF MEMORY SPACE]

        - for Iss test CHEK :
                • check, for each channel, if the Iss current is >=50uA
                • if Iss is NOT >=50uA ⟹ THE CHANNEL IS NOT FUNCTIONING CORRECTLY
        - for INHIBIT and ProbeInput test CHECK :
                • check if the shape of the plotted data of each channel is like a square wave with 50% Duty-cycle
                • if it's NOT like a square wave ⟹ THE CHANNEL IS NOT FUNCTIONING CORRECTLY

        HOW THE CHECK RESULTS OF CHANNEL AND TEST ARE DISPLAYED IN THE REPORT :
                [1] THE REPORT BEGINS WITH RATIOS BETWEEN
                number of channel that passed positively the check/number of channels present
                for each test and for all three togheter (Iss,INHIBIT,ProbeInput and all test togheter)
                [NOTE : notice, there is a fourth row that indicates the channels that PASSED ALL THE TESTS]

                [2] THEN A TABLE WITH ALL THE CHANNELS ON COLUMNS AND ALL THE TESTS ON THE ROWS WILL DISPLAY THE CHECK RESULTS
                (name of the table : TABLE FOR DISPLAY CHECK-RESULT OF CHANNEL AND TESTS)
                [NOTE : as mention in the note of the point [1] there is a fourth row that indicates the channels that PASSED ALL THE THREE TESTS]

                [3] THEN CHECK-RESULTS ARE DISPLAYED IN DETAILS

[WARNING  : THE REPORT GIVE THE CHECK ON THE DATA THAT YOU HAVE TESTED, FROM WHEN YOU OPENED THE GUI TO NOW, AND CHECKS EVEN THE NON YET TESTED.
(this means that if you haven't made yet some of the type of tests available (Iss,INHIBIT,ProbeInput) and for all the channels available,
 you will have faulty check(not valid check result) on those not yet tested)]

|\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/|
```

Figure 3.19: Example of the REPORT file produced after the tests ends

3.5. How the testing board and GUI work together

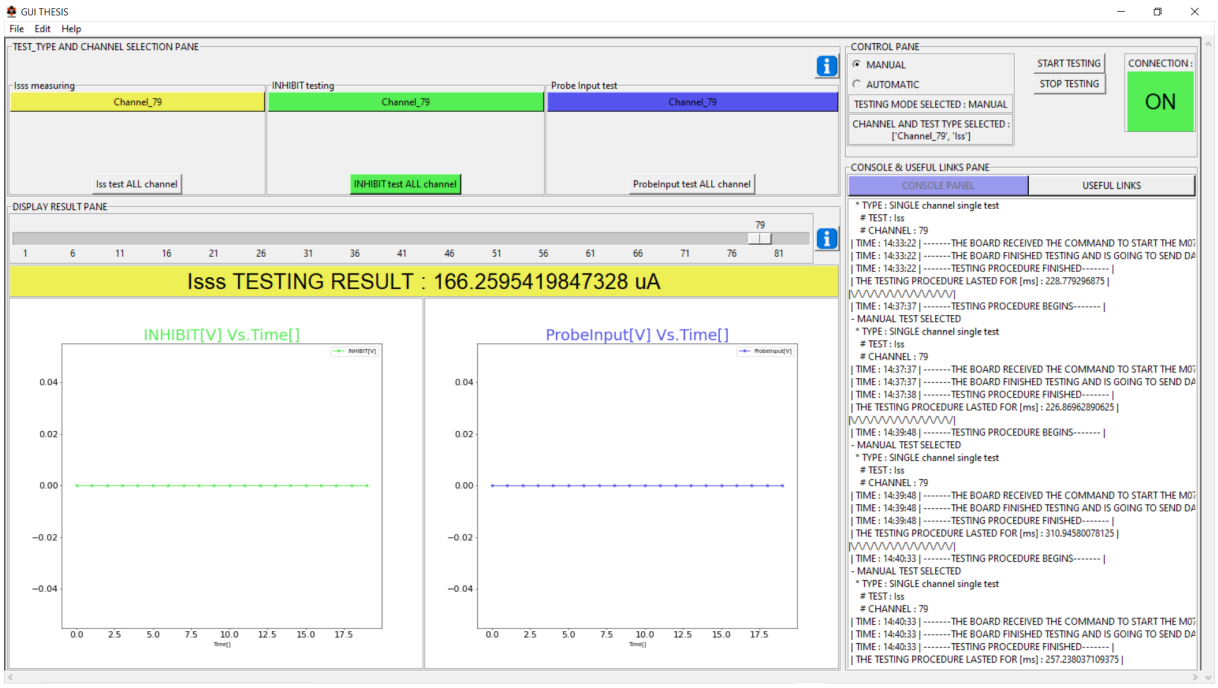


Figure 3.20: Example of the GUI windows after some tests are done and after the selection of the tested channel to be displayed in the Bottom left of the window

The GUI controls the Testing board from the USB connection. The μC handles all the Testing implemented on the board and selects the channel to test. One example of a GUI window during multiple testing and evaluation of the result are present in the Fig.3.20 below.
For the GUI to control the testing board and for the board to send the data collected after the test, a communication protocol on the USB was needed. Furthermore to have more reliability on the test status communication, some sophisticated strategies were developed to avoid any communication error. On the GUI CONSOLE it is possible to see the status of the communication of the testing procedure as I already presented in the Sec.3.4.
Before starting the testing, when the board is USB-connected to the computer, the connection activation between the two is needed and it is done by selecting the bias board into the "SER-PORT CONN. CHOICE" windows (it can be opened in the GUI "file" menu). After the selection of the board the communication of the testing procedure desired can start. First, a check to see if the board is working properly, is given by verifying if the board is currently sending a massage that says **WAIT** (meaning that it is waiting for a test request). If it is working properly a test message can be send to the board. There are different testings messages requests that can be sent to the board and they are: **A0** is for the "AUTOMATIC" test and this means that all the channels are tested for all the three tests type. **M1** is for the test of all the channels for the "I_SSS measurement" test. **M2** is for the test of all the channels for the "INHIBIT test". **M3** is for the test of all the channels for the "Probe-Input test". **M0X**$_{tens}$**X**$_{units}$**Y** is for the test of the **X**$_{tens}$**X**$_{units}$ channel number and for the **Y** test number(e.g. **M0231** is the test of the 23^{rd} channel for the "I_SSS measurement" test). When the board has received the test message it starts the testing procedure selected by first sending back to the GUI the message saying that it has received the testing request (the received acknowledgement message, sent to the GUI, is made by: the test message + **RC**). During testing procedure the board is constantly sending (every 500ms) the **BUSY** message to the GUI to keep a line of communication that says: I am alive and I am currently in the middle of the test. If the GUI does not read the **BUSY** message for at least 2 second, it ends the communication, sends a **STOP** message to the board and writes on the CONSOLE that the board had some problem during testing. Anyways when the board works fine, the **BUSY** message is present, the testing procedure comes to an end and the board sends to the GUI a message, every 500ms, asking to prepare itself to receive the data collected from the test (the message is composed by the test message + **SD**). If the GUI responds in less than 2,5 second to the board with the **SDRC** message (meaning that it has received the message and is ready to receive the data), the board stops the communication procedure for data sending and goes in "idle" mode by restarting to send the **WAIT** message. In the end, if all the steps

went right, the data collected are sent to the GUI and, if the size of the data received is right, the communication and testing procedure ends.

3.6. Characterisation and measurement of the Testing Board and GUI

This section will present the test done with a primitive prototype of the ETTORE board (Fig.3.21) mainly used for the testing of 2 1-pixel SDD and 7-pixel SDD detector in 2017/2018

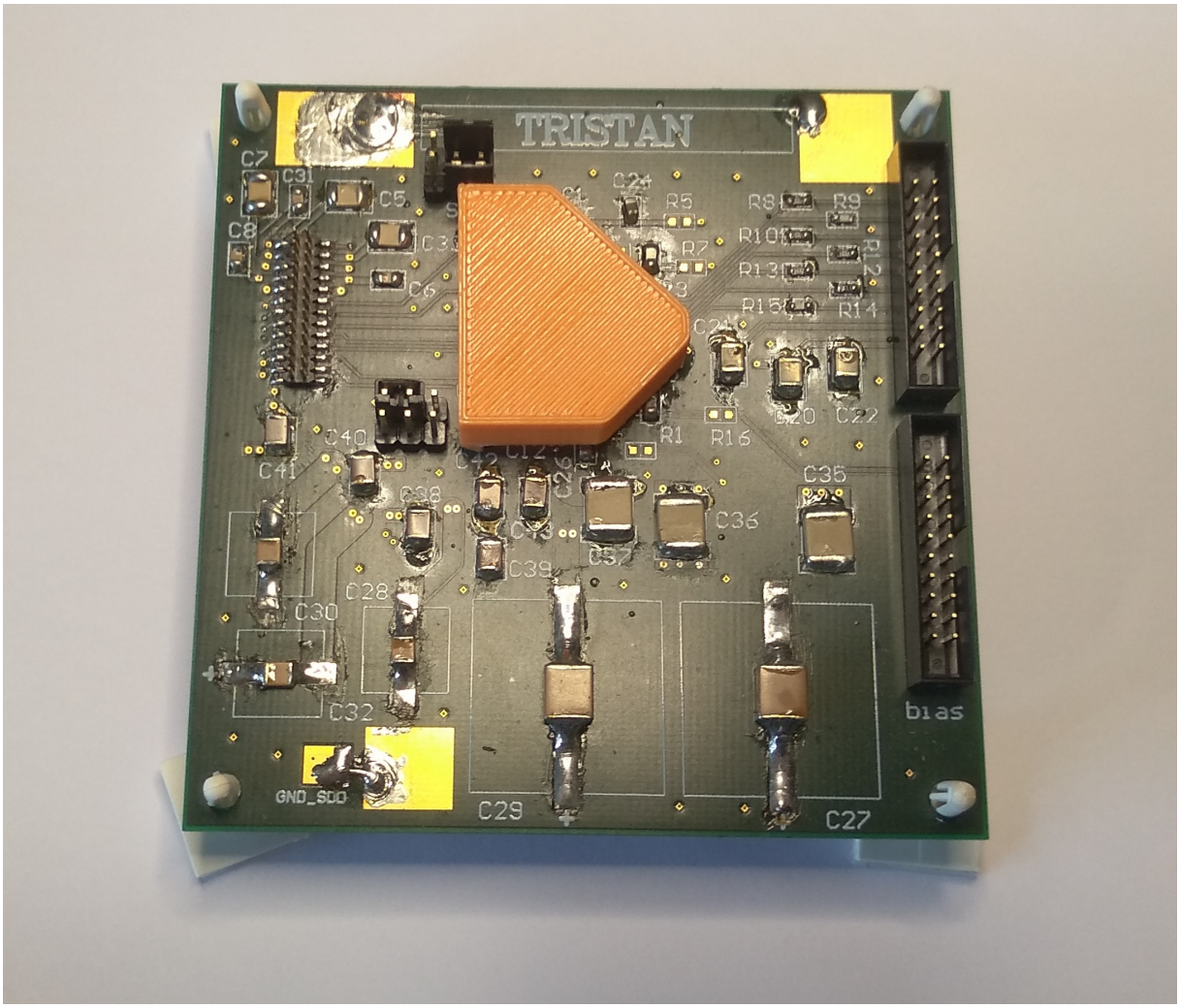


Figure 3.21: ASIC Board developed in Politecnico di Milano for early stages of the TRISTAN project. it is able to test multi-SDD detectors from 1 to 7 pixel size

This first Fig.3.22 down below represent the flying connection needed to connect one

channel of the testing board to one channel of the old version ETTORE board. *(Note: the connection points on the old ETTORE board had the possibility to switch between two different channels of the even ASIC old version. One of the two channels has a faster response compared to the other. The selection between the two is possible through the two jumpers on the 2 6-pin headers near the orange ASIC cover).*

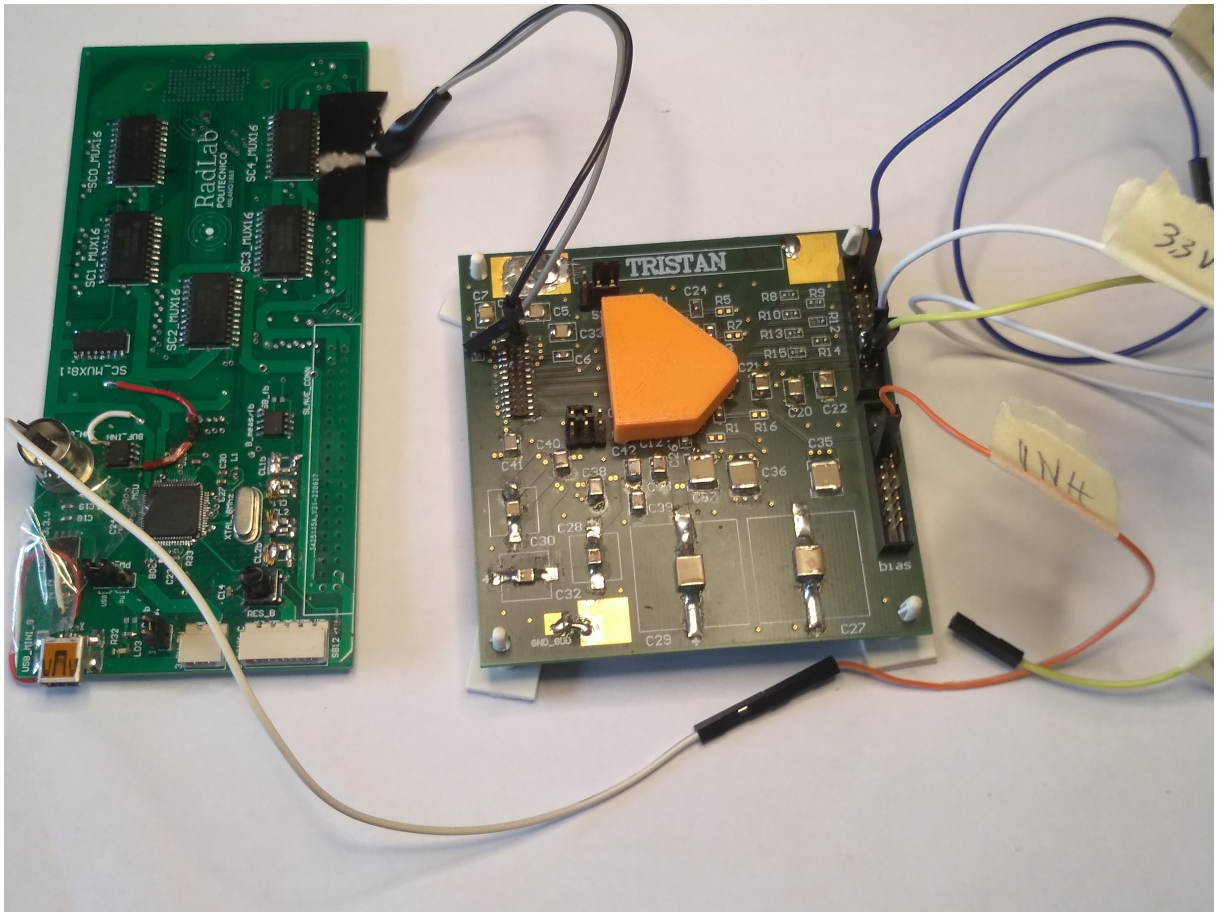


Figure 3.22: Setup with flying connection between the testing board and the old version ASIC board (Fig.3.21)

Now, after all the discussion on the ASICs and on its board (Chapter2), it should be clear that the ASIC board needs to receive powering and biasing source for the ASIC and for the detector. Consequently, the power sources for the ASIC have been connected (V_{DD} = 3,3V V_{SSS} = (0V to -10V) and GND) as in Fig.3.23 below. The testing board instead is getting the power from the PC through the USB connection and farther the USB connection allow the communication with the GUI (as already discussed in Sec.3.5).

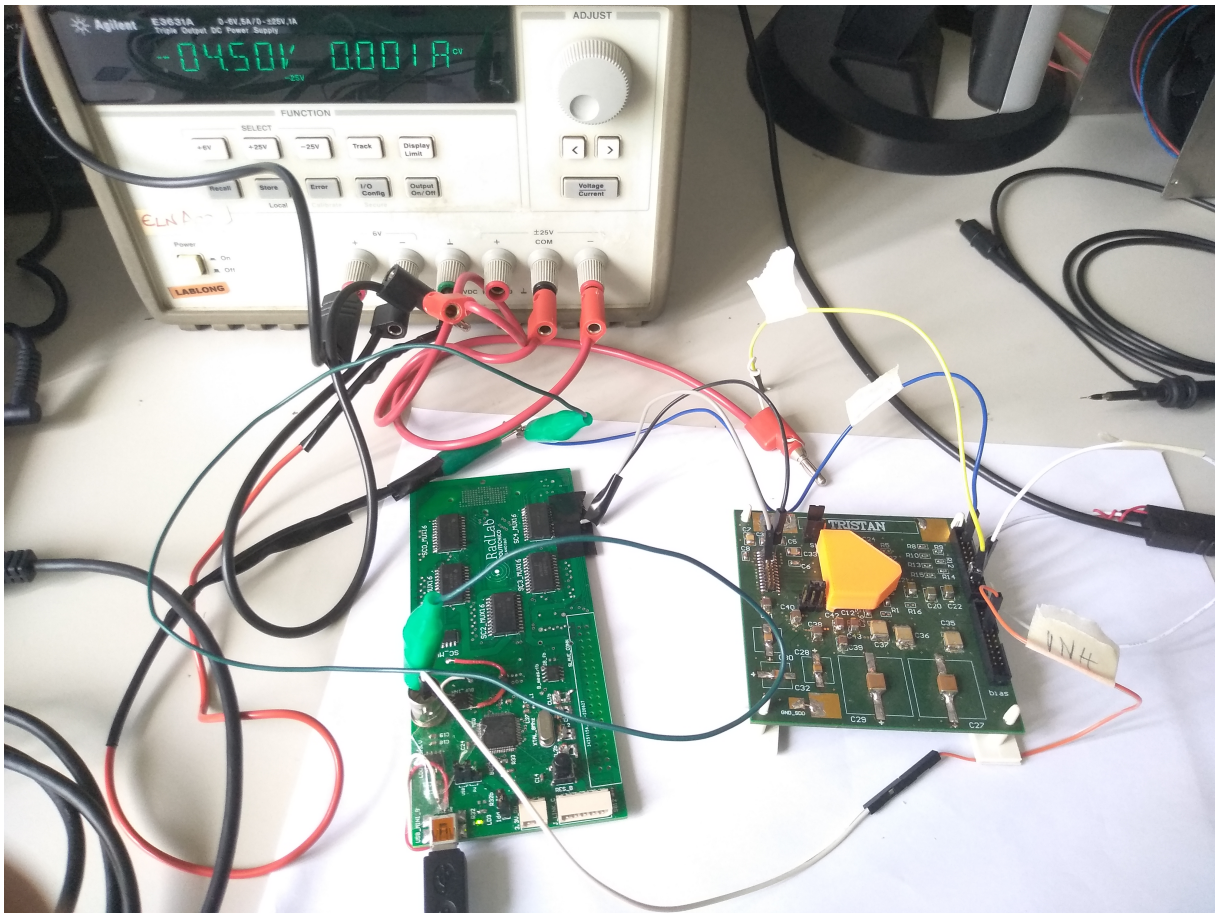


Figure 3.23: Setup with the PC, the power source and the flying connection between the testing board and the old version ASIC board (Fig.3.21).

The tests were done only on the 79^{th} channel connected with fling wires to the ASIC channel. I have tried the slow channel of the ASIC and the measurement results were not precise. Instead the fast response channel of the ASIC gave quite promising results. I started trying only the "I_SSS measurement" and no differences were registered from one measurement result to another. Since there is great repeatability of the measured results, I tried to change the I_SSS given by the ASIC channel by changing the biasing voltage of V_{SSS} starting from 0V and with little step at a time going to more negative potentials. Every result was taken at least three times and the same value came out. The I_SSS measured values dependence to V_{SSS} were coherent with the polarization current circuit theoretical behavior at the **SC** pin of the ASIC channel. All the measured results are in the Table3.1 below. This good results made me think that the problem with the slow ASIC channel was probably a consequence of the too fast testing procedure of my board that did not allow the channel to reach its electrical working (static) point.

Measured I_{SSS} vs. V_{SSS}

	I_{sss}.*
$V_{sss} = 0V$	0μA
$V_{sss} = -1V$	40.3μA
$V_{sss} = -3V$	176.3μA
$V_{sss} = -4V$	229.2μA
$V_{sss} = -4.5V$	256.9μA
$V_{sss} = -5V$	284.6μA
$V_{sss} = -5.5V$	309.8μA

Table 3.1: The polarization current of the JFET (I_{sss}) with varying V_{sss} (nominal range is from 0V to $-10V$) is measured on the old ASIC board by the Testing board (Fig.3.23). Since the board is not suited to handle voltages lower than zero (would be the case if I_{sss} become greater then 330μA), I did not push, to lower V_{sss}, to avoid risking to exceed the testing board limitation. ((*) every measurement was done with the 79^{th} channel of the testing board at least 3 times and the results were always the same)

Some problem is affecting the "INHIBIT test" and the "Probe-Input test": This is because the results coming from the "INHIBIT test" sometimes seemed right and some other times not and for the "Probe-Input test" no response was detected. The 3.3V saturation of the output, of the ASIC channel, has been always detected by the testing board as it was predicted in Sec.3.1. In the future a deeper analysis and trial on the testing board could find and solve all the problems.

4 | Conclusions and future developments of the testing board and GUI

In this final chapter a recall on the future development of the TRISTAN project is given. Instead the future of the testing board and GUI are described focusing on possible advancement to test other stages in the TRISTAN acquisition system. There is even a discussion on the current problem and possible solutions for the board..

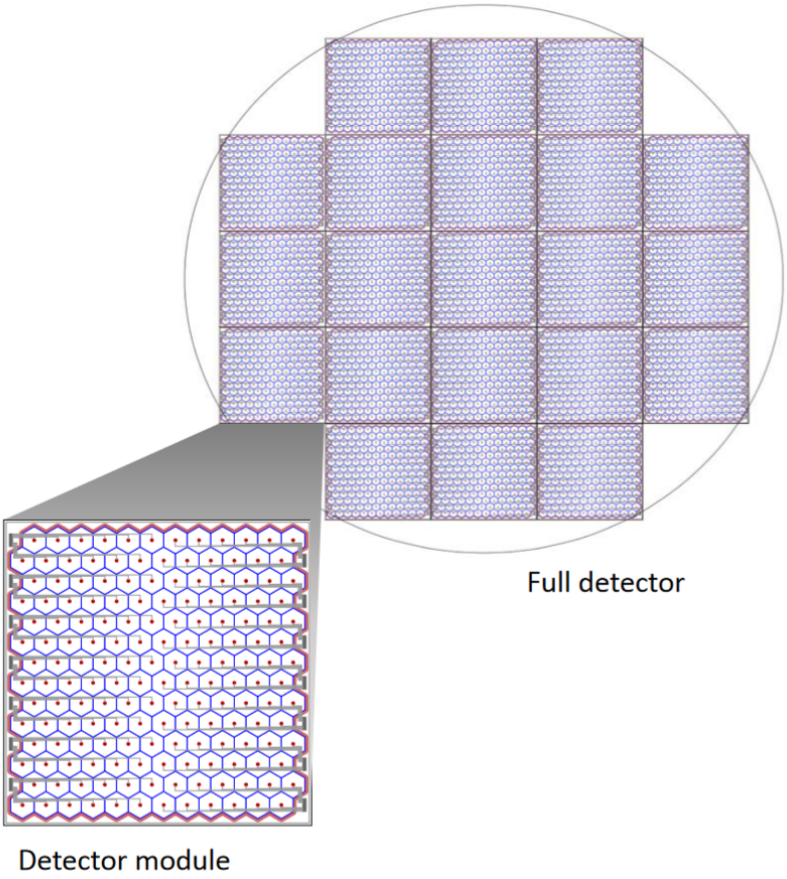


Figure 4.1: Schematic view of the finale 21 166-pixel detectors module

The Future of the TRISTAN project was already envisioned in the SubSec.1.2.2 where the KATRIN project showed the need to have a mixing amplitude ($\sin^2\theta$), of the sterile neutrino with the active Standard Model electron neutrino, with statistical sensitivity that can reach a region of cosmological interest. The TRISTAN project is the solution for the KATRIN beamline to reach such high sensitivity. I already presented in SubSec.1.2.2 the Phase-1 with 9 166-pixels detectors module for the first stage of TRISTAN operation. Then in the Phase-2 the TRISTAN detector is operated with 21 166-pixel detectors module 4.1. In Fig,1.6 it is represented the KATRIN sensitivity to keV-scale sterile neutrinos for the different TRISTAN Phases scenarios.

For what regards the Testing board, something does not seem to be working properly. It was already stated in Sec.3.6, where it was presented the characterisation of the testing board, that only part of the testing procedure was working fine. One of the possible causes could be the fact that the testing procedure does not allow all the tests to be done on an electrical working (static) point, as the tests were developed to do. Consequently if this is the problem, by delaying the testing on each channel for each test, all the system should work. Since the testing procedure required a maximum time of 400ms and most of the time is taken by the communication protocol, an increase of some *ms* for each channel and for each test would increase the testing time to about 1-2 *second* (which could be an absolutely fine solution). Another possible problem, that could justify the non-functioning testing procedures, could be related to some wrong circuit project or design that obviously needs to be found first, if present, and then to be evaluated.
The future for the testing board with other expansion board controlled through the 40-pin ribbon connector has various possibilities. The ribbon connector has 3 pin with 3,3V and other 3 pin with GND, and all the other 34-pins are connected to the still free pins of the μC. This allows the connection to one or more slave boards. This would enable the testing of other parts of the acquisition system. One of the important parts is the channels output from the ETTORE board to the DAQ. It could have problems of manufacturing with malfunctioning probability similar to the channel lines on the detector side of the ASIC board. Implementing changes on the GUI and on the μC firmware, to allow the addition of a slave board, could be difficult. However, from the GUI point of view, there is the need to create new test selection buttons inside the top left pane and there is plenty of space to accommodate it. The display of another test data in the bottom left pane could lead to a lack of space, but it would still be feasible by increasing enough the pane size. The list containing all the test results needs to consider the new space required for the new test. The Report text-file needs to implement the check on the new test results

and the display of them. The protocol needs to have a new function for the collection of the data and to add a new message to request to the board the new test type. The last point is valid even for the communication protocol in the μC firmware that needs to handle the new test request. The firmware needs to implement the new testing procedure function and the sending of the data function (that highly depends on the size of data). I would say that without a good knowledge of the GUI and the firmware in the μC, this task could be quite hard and it would probably require a learning process of some of the functions already implemented.

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